

DAC/ISSCC Student Design Contest Guidelines for Submission

The Student Design Contest is sponsored by the Design Automation Conference (DAC) and the International Solid State Circuits Conference (ISSCC) to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges.

Criteria for entering the Contest

Submissions are invited from full-time graduate and undergraduate students. The design must have taken place as part of the students' course or research work at the university and must have been completed within 18 months prior to the submission deadline: Friday December 21, 2002

Designs can be for analog, digital, or programmable circuits and systems. Submissions can be embodied as integrated circuits, reconfigurable processors, SoCs, platform-based or embedded systems designs.

Examples include:

- Analog Integrated Circuits
- Digital Integrated Circuits
- FPGA based designs
- Reconfigurable Processors
- SoC / Platform-based designs
- Embedded Systems
- MEMS/Optics/Bio-Chips

The contest allows entries of both integrated circuits and electronic systems (board-level designs). It will have prizes in two categories: Operational (built and tested) and Conceptual (designed and simulated). Operational designs will have been built and tested. Proof of implementation in the form of die- or board-photographs and measurement data must be supplied. Conceptual designs need not have been implemented but must have been thoroughly simulated and must include a test plan.

While the project must fall into one of the two categories above, the project can originate from either

- Undergraduate Class Work
- Graduate Class Work
- Graduate Research Work

Students will submit write ups of their designs, up to 4,000 words and 10 figures. They will be evaluated on the following criteria:

- Motivation/Justification (Why was this done?)
- Description of the design process (How was this done?)
- Functional description of final project (How does it work?)
- Physical description, size, speed, power etc. (How well does it perform?)

- Testing strategy and results (Simulation for Conceptual category) (Did it work?)

Submitting a Design

Submission will be in the DAC paper format, and will be done electronically via the DAC web site. Submissions will include two files: the title and a 60-word abstract; and a document describing the design, not to exceed 4000 words. The deadline for submission is December 21, 2002. Please refer to the DAC web site, "Call for Papers," for additional information.

It will be appropriate for a professor to be included as a co-author if he/she was instrumental in your approach to the design, or provided other guidance that contributed to the success of your design.

Judging and Suggestions for Designers

A panel of experts from industry and academia will judge submissions. Judging criteria will include originality, soundness of engineering, measured performance and the quality of the written submission.

Awards will be given at a luncheon at the Design Automation Conference in June.

Writing style should be clear and concise. Remember that the judges' expertise may not be in the area of your project. Make your explanations straightforward and understandable.

Design for testability is important. Discuss testing issues you have considered in the design and approaches you took or will take in testing. Engineering specifications and performance statistics can be efficiently presented in tabular form.

You may want to address some of the following questions and issues in your written report:

System Overview:

- Motivation for designing the chip or system.
- Is the implementation medium appropriate?
- Does this design satisfy the system requirements?
- What is unique about this project?
- What novel ideas or elegant solutions does the design include?

Implementation and engineering considerations:

- Specifications: functional, timing, electrical, and environmental (temperature).
- Trade-offs: architectural and circuit trade-offs, I/O considerations, floor-planning and interconnect approaches. Emphasis should be placed on why you did what you did.
- Timing and Critical Paths. What clocking scheme is used? Why?
- Which paths are critical? Have you simulated or measured their delays?

Block Diagram, Logic / Circuit Diagrams, and Algorithms.

Photo or Final Layout Plot (annotate so various blocks can be identified).

Verification/Simulation (keep it brief): how did you assure that the chip would work as specified?

Testing:

How did you, or will you, test this part with I/O pins only?

What test equipment did you use?

Actual test results, if available, should be summarized.

Statistics:

Die size, total power, number of transistors, density of layout, maximum clock speed, etc.

Contest Awards

The total prize money is expected to be around \$15,000, shared between 1st, 2nd, and 3rd, place winners in each of two categories "conceptual" and "operational". Winners of awards will be notified prior to the conference and offered travel assistance to attend the conference. Winning submissions will be displayed as posters at DAC at the University Booth on the show floor. Selected winning entries may be included in the technical program at the discretion of the technical program committee. This year, for first time, winners will also be invited to a special poster session at ISSCC 2004.