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**DESIGN AUTOMATION CONFERENCE SET TO DELIVER ROBUST TECHNICAL PROGRAM IN CELEBRATION OF 40<sup>TH</sup> ANNIVERSARY**

*Power Management Design Issues Among Major Conference Program Topics*

**BOULDER, Colo. – March 17, 2003** – The 40th Design Automation Conference (DAC) today announced a strong technical program for its annual conference to be held June 2-6 at the Anaheim Convention Center, Anaheim, California. In addition to its traditionally diverse and expansive program, this year's new elements include an increased emphasis on power management design issues, eight DAC Pavilion panels, two "Best of International Solid-State Circuits Conference" special sessions, and an expanded Hands-on Tutorials program.

"With a record number of technical papers and panel submissions—a 30 percent increase from last year—DAC is proud to announce another solid program, offering attendees an even greater opportunity to learn and experience the latest trends, tools and design methodologies in the industry," said Ian Getreu, 40th DAC general chair. "Our goal is to ensure that we deliver the most up-to-date program content that can be applied to current design challenges. This year's focus will emphasize power management methodologies and tools in addition to embedded systems and other pressing design issues."

More than 10,000 participants are expected to attend this year's conference, which will showcase more than 170 exhibiting companies and over 200 papers, panels, sessions and tutorials. The conference also will feature two dynamic keynote speakers, as well as various workshops.

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Conference attendees will have an opportunity to get up-to-the-minute information on design technology and methodologies that impact their current design processes. For instance, on Monday attendees can participate in the “Design Techniques for Power Reduction” tutorial, the “Introduction to Chips and EDA for a Non-Technical Audience” workshop, and a DAC Pavilion panel titled “Semiconductor IP Business: Is It Real?”

Tuesday’s highlights include the keynote address by Sir Robin Saxby, executive chairman of ARM, a special session on “Real Challenges and Solutions for Validating Systems-on-Chip,” a panel on “Reshaping EDA for Power,” and a DAC Pavilion panel discussing “EDA Business Forecast Highlights.”

Wednesday offers attendees an IEEE Design & Test feature panel addressing “Cheap Submicron: The Next Implementation Fabric,” a special session titled “Coping with Variability: The End of Domestic Design,” a DAC Pavilion panel discussion on “Platforms: Yes, But What Type is Best?” and a special session focusing on “How Application/Technology Evolutions will Shape Classical EDA.”

Thursday choices include a panel titled “Libraries: Lifejacket or Straightjacket?” and a retrospective keynote address by Alberto Sangiovanni-Vincentelli, professor of Electrical Engineering and Computer Sciences at University of California at Berkeley, as well as an ISSCC special session titled “The Design of State-of-the-Art Microprocessors.”

Friday offers five full-day tutorials, including “Design for Manufacturing in the Sub-100nm Era” and “Assertion-Based Verification.”

The attached addendum provides more detail on conference highlights. For more information on this year’s technical program also visit DAC’s Web site at [www.dac.com](http://www.dac.com).

### **Registration**

To register for DAC, visit [www.dac.com](http://www.dac.com) or call 800-321-4573 in the U.S. to request registration materials. The advance conference registration discount deadline is May 5, 2003.

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## **About DAC**

DAC is the premier forum for the electronic design industry to exchange information on products, methodologies, and processes. Attended by more than 10,000 developers, designers, researchers, managers, and engineers from leading electronics companies and universities around the world, DAC includes more than 170 exhibitors and offers a robust technical program covering the electronics industry's hottest trends.

The conference is sponsored by the Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA), the Institute of Electrical and Electronics Engineers/Circuits and Systems Society (IEEE/CAS) and the Electronic Design Automation Consortium (EDA Consortium). For more information, including registration, visit the DAC Web site at [www.dac.com](http://www.dac.com), or contact DAC management at 800-321-4573.

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## **Addendum**

### **40<sup>th</sup> DAC Highlights**

#### **Low Power Design Highlights**

Sessions, panels and hands-on tutorials containing over 70 papers will be presented under various power analysis topics including:

- Seven Hands-on Tutorials on “Signal and Power Integrity”
- “Design Techniques for Power Reduction” (Tutorial 1)
- “Reshaping EDA for Power” (session 2)
- “Power Grid Analysis and Optimization” (session 8)
- “Low-Power Embedded Systems Design” (session 9)
- “Managing Leakage Power” (session 11)
- “Architectural Power Estimation and Optimization” (session 36)
- “Energy-Aware System Design” (session 52)

#### **“Best of ISSCC Papers” Highlights**

DAC will offer two special sessions with some of the best papers from the 2003 International Solid-State Circuits Conference (ISSCC), which illustrate how state-of-the-art microprocessors and systems-on-chip are designed to solve issues in design convergence and signal integrity. Topics include:

- “High-Speed Heterogenous Design Techniques” (session 40)
- “The Design of State-of-the-Art Microprocessors” (session 41)

#### **Panel Session Highlights**

Eight panel sessions with guests ranging from chief executive officers to academic professors will offer ample debate and discussion. Panel topics include:

- “Reshaping EDA for Power” (session 2)
- “COT: Customer Owned Trouble?” (session 7)
- “Emerging Markets: Design Goes Global” (session 12)
- “Mixed-Signals on Mixed Signal: The Right Next Technology” (session 17)
- “Cheap Submicron: The Next Implementation Fabric” (session 22)
- “Nanometer Design: Place Your Bets” (session 32)
- “Libraries: Lifejacket or Straightjacket?” (session 37)
- “Formal Verification: Prove It or Pitch It” (session 42)

#### **Special Session Highlights**

Seven special sessions in the technical program will feature invited presentations by leading scholars and engineers. The topics cover:

- “Real Challenges and Solutions for Validating Systems-on-Chip” (session 1)
- “Emerging Design and Tool Challenges in RF and Wireless Applications” (session 6)
- “Nano Technology: Design Implications and CAD Challenges” (session 16)
- “Coping with Variability: The End of Domestic Design” (session 21)
- “How Application/Technology Evolutions will Shape Classical EDA” (session 26)
- “ASIC Design in the Nanometer Era: Dead or Alive?” (session 46)
- “Design Automation for Quantum Circuits” (session 51)

## **Keynote Speakers**

On Tuesday, June 3, Sir Robin Saxby, executive chairman of ARM, will deliver the opening keynote address entitled “Less than 100nm ... A Giant Leap for Mankind?” Thursday’s keynote will feature Alberto Sangiovanni-Vincentelli, professor of Electrical Engineering and Computer Sciences at University of California at Berkeley, who will present “The Tides of EDA” (see separate press release distributed March 3, 2003).

## **DAC Pavilion Panels**

The second annual DAC Pavilion will broadcast live portions of the technical program on the exhibit floor. Pavilion-exclusive panel sessions will also offer attendees the opportunity to participate in panel debates, view live broadcasts of selected technical sessions and keynotes, and relax in the lounge. Some topics include:

- Managing Mask Costs
- Semiconductor IP Business: Is It Real?
- Ask the CTO
- Student Design Contest Awards
- ARM Twisting: Ask Sir Robin
- EDA Business Forecast Highlights
- Wall Street’s View of EDA: The 2003 Update
- Platforms: Yes, But What Type is Best?

## **Best Paper Awards**

Technical papers to be presented at this year’s DAC include topics covering system-level design, synthesis, physical design, verification, power, and IP issues. Best Paper Awards in the amount of \$1,000 each will be announced at the keynote on Thursday, June 5, in the following categories:

- Design, Synthesis, Test and Validation
- Analog/RF/Electrical Modeling, Physical Design and Simulation
- Embedded Systems
- Power

## **Workshops**

On Monday, June 2, DAC will host the “Introduction to Chips and EDA Workshop” which is targeted to non-technical people. The “Interoperability Workshop,” which addresses interoperability challenges facing the electronics industry, will take place on Monday, as will the highly popular “Workshop for Women in Design Automation.”

## **Full-Day Tutorials**

This year’s full-day tutorial lineup includes “Design Techniques for Power Reduction” and will be held on Monday, June 2. This tutorial will cover techniques for reducing active and standby power consumption in desktop and portable devices. Other full-day tutorials, scheduled for Friday, June 6, include:

- System-on-Chip Test Strategies
- Design for Manufacturing in the Sub-100nm Era
- Assertion-Based Verification
- Assembling an SoC: Communication Architectures and Protocols
- High-Performance ASIC Design