



Tuesday, June 10

9:15 to 10:15

General Session and Keynote Speaker

Scott G. McNealy - President, Sun Microsystems, Inc. Mountain View, CA
Opening Remarks • Awards • Keynote Address (Room - Arena)

Break

10:30 to 12:00

CEO PLENARY PANEL: The Executive View of the EDA Industry

no badge required (Room - Arena)

Lunch

2:00 to 4:00

- 1. Sequential Synthesis Rm B7
- 2. Interconnect Modeling Rm B8
- 3. Novel Techniques for Software Scheduling Rm A6/A7

- 4. ***-Panel:** Low-Power Design Tools: Where is the Impact? Rm A1
- 5. Simulation Techniques for Microprocessors Rm A9/A10

Break

4:30 to 6:00

- 6. Combinational Logic Synthesis Rm B7
- 7. Interconnect Parasitic Extraction Rm B8
- 8. ***-Advances in Timing Analysis for Embedded Software** Rm A6/A7

- 9. Applications of Formal Verification Rm A1
- 10. System-Level Exploration and Refinement Rm A9/A10

Party

6:00 to 7:00

DAC Cocktail Party at the Anaheim Marriott

Wednesday, June 11

8:30 to 10:00

- 11. Binary Decision Diagrams Rm B7
- 12. Timing Analysis Rm B8
- 13. **** -Retargetable Code Generation for Core Processors** Rm A6/A7

- 14. ***-Panel:** Low-Power Design Tools: Where is the Impact? Rm A1
- 15. Simulation Techniques for Microprocessors Rm A9/A10

Break

10:30 to 12:00

- 16. ***-Formal Verification** Rm B7
- 17. Analog Simulation Rm B8
- 18. Software Synthesis for Embedded Systems Rm A6/A7

- 19. Experiences in System Design and Education at Universities Rm A1
- 20. Standard Cell and Physical Design Methods Rm A9/A10

Lunch

2:00 to 4:00

- 21. Modeling and Transformations in Synthesis Rm B7
- 22. Statistical Power Estimation Techniques Rm B8
- 23. ***-Co-Simulation** Rm A6/A7

- 24. **Panel:** Challenges in Worldwide IP Reuse Rm A1
- 25. Emerging Technologies and Architectures for Low Power Rm A9/A10

Exhibit Hours 10:00AM–6:00PM / Demo Suite Hours 8:00AM–9:00PM

*-Tutorial Included /
**-Full Tutorial Session

Wednesday, June 11 (cont.)

 4:30 to
6:00

- 26. High Level Synthesis for Low Power Rm B7
- 27. *-Module Generation Rm B8
- 28. BIST and DFT Rm A6/A7

- 29. **Panel:** Hardware/Software Co-Verification Rm A1
- 30. DSP & Telecommunication System Design Rm A9/A10

 7:30 to
10:00

DAC Wednesday Night Southern California Fantasy Party

Thursday, June 12

 8:30 to
10:00

- 31. ** -High Level Power Modeling, Estimation and Optimization Rm B7
- 32. Advances in Partitioning Rm B8
- 33. Processor Test Techniques Rm A6/A7

- 34. **Panel:** The Next Generation HDL Rm A1
- 35. Design Processes and Frameworks Rm A9/A10

Break

 10:30 to
12:00

- 36. Probabilistic Models of Input Data for Efficient Power Estimation Rm B7
- 37. Hot Topics in Routing Rm B8
- 38. Test Generation and Fault Simulation Rm A6/A7

- 39. **Panel:** The Road Ahead in CPLD & FPGA Design Methodology Rm A1
- 40. Deep Submicron Modeling and Analysis Rm A9/A10

Lunch

 1:00 to
1:45

Keynote Speaker: Michael A. Aymar
Vice-President / General Manager Intel Corp., Santa Clara, CA Rm A1

 2:00 to
4:00

- 41. Technology-Dependent Optimization for Performance and Power Rm B7
- 42. *-CAD Issues for Micro-Electro-Mechanical Systems Rm B8
- 43. Hardware/Software Partitioning Rm A6/A7

- 44. *-**Panel:** Noise and Signal Integrity in Deep Submicron Design Rm A1
- 45. Designing High Performance and Low Power Microprocessors Using Full Custom Techniques Rm A9/A10

 4:30 to
6:00

- 46. Formal Verification Techniques Rm B7
- 47. Placement Techniques Rm B8

- 48. **Plenary Panel:** The EDA Startup Experience: Financing the Venture
no badge required Rm A1

- 49. Heterogeneous System

Demo Suite Hours 8:00AM-5:00PM



2:00
to
4:00

Session 1: Sequential Synthesis

Room B7

*Chair: Richard L. Rudell
Synopsys, Inc., Mountain View, CA
Organizers: Fabio Somenzi, Sharad Malik*

This session considers analysis and optimization problems for synchronous and asynchronous sequential circuits targeting High performance and low power.

1.1 An Improved Algorithm for Minimum-Area Retiming

*Naresh Maheshwari, Sachin Sapatnekar
Iowa State Univ., Ames, IA*

1.2S Efficient Latch Optimization Using Incompatible Sets

*Ellen M. Sentovich, Horia Toma, Gerard Berry
Ecole des Mines de Paris, Sophia-Antipolis,
France*

1.3S Sequence Compaction for Probabilistic Analysis of Sequential and Interacting Finite-State Machines

*Diana Marculescu, Radu Marculescu,
Massoud Pedram
Univ. of S. California, Los Angeles, CA*

1.4 Synthesis of Speed Independent Circuits from STG-Unfolding Segment

*Alexei Semenov, Alexandre Yakovlev
Univ. of Newcastle Upon Tyne, Newcastle Upon
Tyne, UK*

*Enric Pastor, Marco A. Pena, Jordi Cortadella
Univ. Politecnica de Catalunya, Barcelona, Spain*

1.5 Telescopic Units: Increasing the Average Throughput of Pipelined Designs by Adaptive Latency Control

*Luca Benini
Stanford Univ., Stanford, CA
Enrico Macii, Massimo Poncino
Politecnico di Torino, Torino, Italy*

Session 2: Interconnect Modeling

Room B8

*Chair: Lawrence T. Pileggi-Carnegie Mellon Univ.,
Organizers: Andrew T. Yang, Jacob White*

Calculating the impact on performance of interconnect requires generating efficient models which can be used in circuit simulation or analytic analysis. In this session a variety of modeling issues are addressed including: passivity preservation, on-the-fly or hierarchical reduction, and the impact of coupling effects on delay.

2.1 Zeros and Passivity of Arnoldi-Reduced-Order Transfer Functions for Interconnect Networks

*Ibrahim M. Elfadel, David Ling
IBM Corp., Yorktown Heights, NY*

2.2 Preservation of Passivity During RLC Network Reduction via Split Congruence Transformations

*Kevin J. Kerns, Andrew T. Yang
Avant! Corp., Sunnyvale, CA*

2.3 Lumped Interconnect Models via Gaussian Quadrature

*Keith Nabors, T.-T. Fang, H.-W. Chang,
Kenneth S. Kundert
Cadence Design Systems, Inc., San Jose, CA
Jacob K. White
Massachusetts Inst. of Tech., Cambridge, MA*

2.4 Calculating Worst-Case Gate Delays Due To Dominant Capacitance Coupling

*Florentin Dartu, Lawrence T. Pileggi
Carnegie Mellon Univ., Pittsburgh, PA*



Session 3: Room A6/A7 Novel Techniques for Software Scheduling

*Chair: Gaetano Borriello
Univ. of Washington, Seattle, WA
Organizers: Rajesh K. Gupta, Luciano Lavagno*

Scheduling of operation and events is an important issue both in embedded software implementations as well as in the software system models. The first three papers present novel techniques and models to build as well as validate the embedded software schedules. The last paper addresses static versus dynamic creation and scheduling of reactive events for efficient system simulations.

3.1 Schedule Validation for Embedded Reactive Real-Time Systems

Felice Balarin
*Cadence Design Systems, Inc., Berkeley, CA
Alberto Sangiovanni-Vincentelli
Univ. of California, Berkeley, CA*

3.2 Incorporating Imprecise Computation Into System-Level Design of Application-Specific Heterogeneous Multiprocessors

Yosef Gavriel, Tirat-Gefen
*Mentor Graphics Corp., Wilsonville, OR
Diogenes C. Silva, Alice C. Parker
Univ. of S. California, Los Angeles, CA*

3.3 Data Memory Minimisation for Synchronos Data Flow Graphs Emulated on DSP-FPGA Targets

Marleen Ade, Rudy Lauwereins,
J. A. Peperstraete
Katholieke Univ., Heverlee, Belgium

3.4 An Efficient Implementation of Reactivity for Modeling Hardware in the CSYN Synthesis and Simulation Environment

Stan Liao, Steve Tjiang
*Synopsys, Inc., Mountain View, CA
Rajesh K. Gupta
Univ. of California, Irvine, CA*

Session 4: Room A1 Panel: Low-Power Design Tools: Where is the Impact?

*Chair: Jan M. Rabaey
Univ. of California, Berkeley, CA
Organizer: Nanette Collins
Consultant, Boston, MA*

Power dissipation in ICs is rapidly becoming one of the most significant problems in IC design, and this in portables, as well as ASIC and high-performance micorprocessor platforms. In recent years, we have witnessed the emergence of a variety of design methods and design automation tools to keep dissipation within bounds. Following a 30-minute Tutorial, panelists will present differing views on the subject of low-power design tools. This panel, composed of designers, CAD managers and EDA manufacturers, will address compelling issues, including what effectively works and what does not in the real world, and what is needed for the next-generation designs.

4.1 Embedded Tutorial: Tools and Methodologies for Low Power Design

Jerry Frenkil
Sente Inc., Chelmsford, MA

Panel Members:

Bill Bell
Texas Instruments, Dallas, TX
Jerry Frenkil
Sente Inc., Chelmsford, MA
Vassilios Gerousis
Motorola Inc., Tempe, AZ
Massoud Pedram
Univ. of S. California, Los Angeles, CA
Deo Singh
Intel Corp., Santa Clara, CA
Jim Sproch
Synopsys, Inc., Mountain View, CA

Session 5: Room A9/A10 Simulation Techniques for Microprocessors

*Chair: Haruyuki Tago
Toshiba America Electronic Components,
San Jose, CA
Organizers: Haruyuki Tago, Neil Weste*

Complex microprocessors present serious challenges to today's simulation techniques. This session explores novel techniques to improve simulation performance by using C-based strategies and random tests, test procedures for clock generators, and methods for the debugging of complex FPGA systems.

5.1 A C-Based RTL Design Verification Methodology for Complex Microprocessor

Joonseo Yim, Changjae Park, Wooseung Yang, Hunseung Oh, Joonwoo Kim, Heechoul Lee, Yunghei Lee, In-cheol Park, Chong-Min Kyung
Kaist, Taejon, Korea

5.2 Novel Hierarchical Random Simulation Approach for the Verification of S/390 CMOS Multiprocessors

Gerhard Doettling, Jens Leenstra, Bernd Leppla, Hans-Juergen Muenster, Joerg Walter
*IBM Deutschland Entwicklung, Boeblingen, Germany
Kevin Kark, Bruce Wile
IBM Corp., Poughkeepsie, NY*

5.3 Efficient Testing of Clock Regeneratoe Circuits

Rajesh Raina, Robert Bailey
*Motorola, Inc., Austin, TX,
Robert Molyneaux, Charlie Beh
IBM Corp., Austin, TX
Charles Njinda
Advanced Micro Devices, Sunnyvale, CA*

5.4 A Real-Time RTL Engineering-Change Method Supporting On-Line Debugging for Logic-Emulation Applications

Wen-jong Fang, Allen C.H. Wu
*Tsing Hua Univ., Taiwan, Roc
Duan-Ping Chen
Quickturn Design Systems, Inc., Mountain View, CA*



4:30
to
6:00

Session 6: Combinational Logic Synthesis

Room B7

Chair: Hamid Savoj

Cadence Design Systems, Inc., Palo Alto, CA

Organizers: Andreas Kuehlmann, Massoud Pedram

This session covers several topics in combinational logic synthesis. The first paper presents a graph-based approach to optimize two-level and/or circuits. The second paper addresses the problem of extracting and using don't-care information in a hierarchical synthesis methodology. The last two papers present solutions to two classical optimization problems in CAD.

6.1 A Graph-Based Synthesis Algorithm for And/XOR Networks

Yibin Ye, Kaushik Roy

Purdue Univ., W. Lafayette, IN

6.2S Logic Optimization of Designs Containing Black Boxes

Tai-Hung Liu, Khurram Sajid, Adnan Aziz

Univ. of Texas, Austin, TX

Vigyan Singhal

Cadence Design Systems, Inc., Berkeley, CA

6.3S Solving Covering Problems Using LPR-Based Lower Bounds

Stan Liao

Synopsys, Inc., Mountain View, CA

Srinivas Devadas

Massachusetts Inst. of Tech., Cambridge, MA

6.4 Exact Graph Coloring in CAD is not Hard

Olivier R. Coudert

Synopsys, Inc., Mountain View, CA

Session 7: Interconnect Parasitic Extraction

Room B8

Chair: Andrew T. Yang

Avant! Corp., Sunnyvale, CA

Organizers: Jacob White, Jason Cong

The ability to route multiple levels of interconnect in deep submicron technology has made it necessary to develop fast approaches for electromagnetic analysis of very complicated structures. In this session, a variety of approaches to generating fast algorithms are presented including: exploiting hierarchy, sparsifying using analytic techniques, and sparsifying using the singular value decomposition.

7.1 Hierarchical 2-D Field Solution for Capacitance Extraction for VLSI Interconnect Modeling

E. Aykut Dengi

Motorola, Inc., Austin, TX

Ron A. Rohrer

Carnegie Mellon Univ., Pittsburgh, PA

7.2S Bounds for BEM Capacitance Extraction

Michael W. Beattie, Lawrence T. Pileggi

Carnegie Mellon Univ., Pittsburgh, PA

7.3S SPIE: Sparse Peec Inductance Extraction

Zhijiang He, Mustafa Celik, Lawrence T. Pileggi

Carnegie Mellon Univ., Pittsburgh, PA

7.4 A Fast Method of Moments Solver for Efficient Parameter Extraction of MCMs

Sharad Kapur, Jinsong Zhao

Lucent Tech. Bell Labs., Murray Hill, NJ



Session 8: Room A6/A7 Advances in Timing Analysis for Embedded Software

*Chairs: Wendell Baker
Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA
Hiroto Yasuura
Kyushu Univ., Fukuoka, Japan
Organizers: Rajesh K. Gupta, Luciano Lavagno*

Accurate modeling of timing performance of software is important to effective embedded system co-design. The task is complicated by uncertainty in control-flow as well as architectural variations. We begin with a tutorial on latest advances in computing close bounds on worst-case execution time of software with pipelining and cache effects. This is followed by a paper on cache modeling and a paper comparing real-time software analysis techniques for embedded systems.

8.1 Embedded Tutorial: Static Timing Analysis of Embedded Software

*Sharad Malik
Princeton Univ., Princeton, NJ*

8.2S A Task-Level Hierarchical Memory Model for Synthesis of Multiprocessors

*Yanbing Li, Wayne Wolf
Princeton Univ., Princeton, NJ*

8.3S Predicting Timing Behavior in Architectural Design Exploration of Real-Time Embedded Systems

*Rajeshkumar Sambandam
Western Michigan Univ., Kalamazoo, MI
Xiaobo Hu
Univ. of Notre Dame, Notre Dame, IN*

Session 9: Room A1 Applications of Formal Verification

*Chair: Andreas Kuehlmann
IBM Corp., Yorktown Heights, NY
Organizers: Haruyuki Tago, Neil Weste*

While formal verification has received ample attention in recent years, its applicability is still a major concern. This session demonstrates some interesting case studies and applications, including the verification of the PowerPC fixed-point execution unit, contents-addressable memories and modules for the automotive market.

9.1 Formal Verification of a Uperscalar Execution Unit

*Kyle L. Nelson
IBM Corp., Rochester, MN
Alok Jain, Randal E. Bryant
Carnegie Mellon Univ., Pittsburgh, PA*

9.2 Formal Verification of Content Addressable Memories Using Symbolic Trajectory Evaluation

*Manish Pandey, Randal E. Bryant
Carnegie Mellon Univ., Pittsburgh, PA
Richard Raimi, Magdy S. Abadir
Motorola, Inc., Austin, TX*

9.3 Formal Verification of Fire: A Case Study

*Jae-Young Jang
Univ. of Colorado, Boulder, CO
Shaz Qadeer
Univ. of California, Berkeley, CA
Carl Pixley, Matt Kaufmann
Motorola, Inc., Austin, TX*

Session 10: Room A9/A10 System-Level Exploration and Refinement

*Chair: Ivo Bolsens
Imec, Leuven, Belgium
Organizers: Ivo Bolsens, Anders Forsen*

At the earliest design stages some of the most important decisions must be made with early data. These papers present new approaches to the specification, estimation, exploration, and refinement of abstract systems.

10.1 Interfaced-Based Design

*James A. Rowson
Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA
Alberto Sangiovanni-Vincentelli
Univ. of California, Berkeley, CA*

10.2 An Integrated Design Environment for Performance and Dependability Analysis

*Robert H. Klenke, Moshe Meyassed,
James H. Aylor, Barry W. Johnson,
Ramesh Rao, Anup Ghosh
Univ. of Virginia, Charlottesville, VA*

10.3 A Dynamic Design Estimation and Exploration Environment

*Ole Bentz, Jan M. Rabaey, David B. Lidsky
Univ. of California, Berkeley, CA*



8:30
to
10:00

Session 11: Binary Decision Diagrams

Room B7

*Chair: Andreas Kuehlmann - Ibm Corp.,
Yorktown Heights, NY*
*Organizers: Massoud Pedram, Andreas
Kuehlmann*

This session is devoted to binary decision diagrams, which have become a very popular data structure for formal verification and synthesis. The first paper analyses the memory locality behavior of breadth-first and depth-first algorithms. The second paper proposes a new technique that combines variable reordering and function transformation. The last paper discusses an improved algorithm for the minimization of BDDs in the presence of don't care conditions.

11.1 Remembrance of Things Past: Locality and Memory in BDDs

Srilatha Manne, Dirk C. Grunwald, Fabio Somenzi
Univ. of Colorado, Boulder, CO

11.2 Linear Sifting of Decision Diagrams

Christoph Meinel, Thorsten Theobald
Univ. of Trier, Trier, Germany
Fabio Somenzi
Univ. of Colorado, Boulder, CO

11.3 Safe BDD Minimization Using Don't Cares

Youpyo Hong, Peter Beerel
Univ. of S. California, Los Angeles, CA
Jerry R. Burch, Kenneth L. Mcmillan
Cadence Berkeley Labs., Berkeley, CA

Session 12 Timing Analysis

Room: B8

*Chair: Karem A. Sakallah
Univ. of Michigan, Ann Arbor, MI*
Organizers: Karem Sakallah, Sharad Malik

This session addresses three distinct timing issues. The first paper proposes a new approach for optimizing interconnect delay by inserting repeaters at appropriate points. The second paper is concerned with resynthesizing combinational circuits that may contain false paths to meet specified performance goals. The final paper employs Presburger arithmetic (the theory of integers with addition) to solve the timing constraints generated from interface timing diagrams.

12.1 Timing Optimization for Multi-Source NETS: Characterization and Optimal Repeater Insertion

John Lillis
Univ. of California, Berkeley, CA
Chung-Kuan Cheng
Univ. of California at San Diego, La Jolla, CA

12.2 Temporal Flexibility in Combinational Circuits

Yuji Kukimoto, Robert K. Brayton
Univ. of California, Berkeley, CA

12.3 Symbolic Timing Verification of Timing Diagrams

Tod Amon, Taokuan Hu
Southwest Texas State Univ., San Marcos, TX
Gaetano Borriello
Univ. of Washington, Seattle, WA



Session 13 Embedded Tutorial: Retargetable Code Generation for Core Processors

Room: A6/A7

Chair: Rajesh Gupta
Univ. of California, Irvine, CA
Organizer: Giovanni De Micheli

This tutorial will briefly present the trend towards using processor cores in systems-on-silicon. First, it will cover market trends for processor cores, and briefly touch the issues concerning application specific instruction-set processors (ASIPs), application-specific signal processors (ASSPs), soft cores and hard cores. Second, it will describe new code optimization approaches which take the special characteristics of core-processor architectures into account. Eventually, it will present techniques for retargeting compilers to new architectures easily and it will show how compilers can be generated from descriptions of processor architectures.

Presenter:

Peter Marwedel
Univ. of Dortmund, Dortmund, Germany

Session 14 Panel: Physical Design and Synthesis: Merge or Die!

Room: A1

Chair: Massoud Pedram
Univ. of S. California, Los Angeles, CA
Organizer: Massoud Pedram

As IC fabrication capabilities extend down to sub-half-micron, the significance of interconnect delay and power dissipation can no longer be ignored. Existing enhancements to synthesis and physical design tools (such as nonlinear delay modeling, custom wire load models, back annotation of calculated delays, early floorplanning, post-layout re-mapping and resizing) have not been able to solve the problem. It thus remains that tradeoffs in logical and physical domains must be addressed in an integrated fashion. Huge business opportunities will be lost unless more revolutionary changes to design flow are made. This panel of experts will address the current split between logic synthesis and physical design and its effect on the design flow. It will then discuss possibilities for merging the two, or at least bringing them closer together. In particular, issues such as consistent wire load and timing models and algorithms which must be employed across the design flow, EDA standards and common databases to support the integration of layout and synthesis tools, evolving structured design styles that offer lower wiring overhead, interconnect-driven logic synthesis and timing-driven physical design will be discussed. Finally, the panel will seek to highlight challenges and potential pitfalls that lie ahead.

Panel Members:

Richard Bushroe-*SEMATECH, Austin, TX*
Raul Camposano-*Synopsys, Inc., Mountain View, CA*
Giovanni De Micheli-*Stanford Univ., Stanford, CA*
Antun Domic
Cadence Design Systems, Inc., San Jose, CA
Chi-Ping Hsu-*Avant! Corp., Sunnyvale, CA*
Michael Jackson-*Motorola Inc., Austin, TX*

Session 15 System-Level Optimization and Verification

Room: A9/A10

Chair: Phil Duncan
Angeles Design Systems, Santa Monica, CA
Organizers: Ivo Bolsens, James A. Rowsen

Efficient implementations for complex system require optimizations in three main areas: function, memory and timing. Each paper in this session approaches one of these topics from a system level viewpoint.

15.1 Interface Timing Verification Drives System Design

Ajay J. Daga, Peter R. Suaris
Interconnectix, Inc., Portland, OR

15.2 Memory-CPU Size Optimization for Embedded System Designs

Barry Shackleford, Mitsuhiro Yasuda, Etsuko Okushi, Hisao Koizumi
Mitsubishi Electric Corp., Tokyo, Japan
Hiroyuki Tomiyama, Hiroto Yasuura
Kyushu Univ., Fukuoka, Japan

15.3 Methodology for Behavioral Synthesis-Based Algorithm-Level Design Space Exploration: DCT Case Study

Miodrag M. Potkonjak
Univ. of California, Los Angeles, CA
Kyosun Kim, Ramesh Karri
Univ. of Massachusetts, Amherst, MA



10:30
to
12:00

Session 16 Formal Verification

Room: B7

*Chair: Fabio Somenzi
Univ. of Colorado, Boulder, CO
Organizers: Fabio Somenzi, Giovanni De Micheli*

This session presents practical, successful formal verification techniques through a tutorial and a technical paper. The tutorial concentrates on the model checking, while the regular paper describes an industrial combinational verifier.

16.1 Embedded Tutorial: Formal Verification in a Commercial Setting

Robert Kurshan
Lucent Tech. Bell Labs., Murray Hill, NJ

16.2 Equivalence Checking Using Cuts and Heaps

Andreas Kuehlmann, Florian Krohm
IBM Corp., Yorktown Heights, NY

Session 17 Analog Simulation

Room: B8

*Chair: Giorgio Casinovi
Georgia Inst. of Tech., Atlanta, GA
Organizers: Jacob White, Hidetoshi Onodera*

The recent explosion in single-chip signal processing systems has renewed interest in techniques for analog simulation. In this session new techniques are described for simulating performance and faults in communication and filtering circuits used in signal processing applications.

17.1 Time-Domain and Mixed Frequency-Time Algorithms for Strongly Nonlinear Circuits With Multi-Tone Excitations

J.S. Roychowdhury
Lucent Tech. Bell Labs., Murray Hill, NJ

17.2 Rapid Frequency-Domain Analog Fault Simulation Under Parameter Tolerances

Michael W. Tian, Richard Shi
Univ. of Iowa, Iowa City, IA

17.3 Swittest: Automatic Switch-Level Fault Simulation and Test Evaluation of Switched-Capacitor Systems

Salvador Mir, Adoracion Rueda, Eduardo J. Peralias, J.L. Huertas
CNM/Univ. De Sevilla, Sevilla, Spain
T. Olbrich
AMS, Unterpemstaetten, Austria



Session 18 Room: A6/A7 Software Synthesis for Embedded Systems

*Chair: Sharad Malik
Princeton Univ., Princeton, NJ
Organizers: Sharad Malik, Luciano
Lavagno*

Synthesis of embedded software spans issues from efficient generation of data-storage to code generation for retargetability. The first two papers in this session address the issue of code generation for digital signal processors that perform an efficient utilization of on-chip address registers and fixed point operation. The last two papers focus on modeling processor architectures for retargetable code generation.

18.1 Analysis and Evaluation of Address Arithmetic Capabilities in Custom DSP Architectures

*Ashok Sudarsanam
Princeton Univ., Princeton, NJ
Stan Liao
Synopsys, Inc., Mountain View, CA
Srinivas Devadas
Massachusetts Inst. of Tech., Cambridge, MA*

18.2 System Level Fixed-Point Design Based on an Interpolative Approach

*Markus Willems, Volker Buersgens,
Heinrich Meyr
Aachen Univ. of Tech., Aachen, Germany*

18.3S ISDL: An Instruction Set Description Language for Retargetability

*George Hadjiyiannis, Silvina Hanono,
Srinivas Devadas
Massachusetts Inst. of Tech., Cambridge, MA*

18.4S Generation of Software Tools From Processor Descriptions for Hardware/Software CoDesign

*James A. Rowson, Mark Hartoog,
Prakash Redd
Alta Group of Cadence Design Systems, Inc.,
Sunnyvale, CA*

Session 19 Room: A1 Experiences in System Design and Education at Universities

*Chairs: Jan M. Rabaey
Univ. of California, Berkeley, CA
Anantha Chandrakasan
Massachusetts Inst. of Tech., Cambridge, MA
Organizer: Jan M. Rabaey*

As integrated systems are getting more complex and diverse, educational institutes face a number of important questions that may have a profound impact on future curricula and research. Does "education for system design" really make sense and what does it entail; How to deal with complexity and scale in university research; What does industry expect from the future generation of design engineers? All these questions will be addressed in this session which features some of the most prominent university experimenters and researchers in the system field, and which reviews some of the largest university system design projects in recent years.

19.1 Education for the Deep-Submicron Age: Business as Usual?

*Hugo De Man
Imec, Leuven, Belgium*

19.2 Infopad: An Experiment in System-Level Design and Integration

*Robert W. Brodersen
Univ. of California, Berkeley, CA*

19.3 Very Rapid Prototyping of Wearable Computers: A Case Study of Custom Versus Off-the-Shelf Design Methodologies

*Asim Smailagic, Daniel P. Siewiorek,
Richard Martin, John Stivorc,
Chris Kasabach
Carnegie Mellon Univ., Pittsburgh, PA*

Session 20 Room: A9/A10 Standard Cell and Physical Design Methods

*Chair: Neil Weste
Macquarie Univ., Sydney, Australia
Organizers: Neil Weste, Randolph E. Harr*

Design methods for dealing with the physical and behavioral design of integrated circuits with a focus on standard cells are presented in this session. The first paper examines, in a general manner, the interface between design and manufacturing at the layout level. Following this, two papers present experiences in the automatic generation of standard cells. The final paper presents an algorithm that can be used to optimize characterization tables for standard cell libraries.

20.1 Design-Manufacturing Interface: Tools

*H.T. Heineken, Jitendra Khare, Wojciech Maly, Pranab K. Nag, C. Ouyang, W. Pleskacz
Carnegie Mellon Univ., Pittsburgh, PA*

20.2 Cellerity - A Fully Automatic Layout Synthesis System for Standard Cell Libraries

*Mohan Guruswamy, Venkat Chiluvuri,
Daniel Dulitz, Andrea Fernandez, Bob Maziasz, Srilata Raman, Larry Jones
Motorola, Austin, TX*

20.3S Developing a Concurrent Methodology for Standard-Cell Library Generation

*Donald G. Baltus, Thomas Varga, Robert Armstrong
LSI Logic Corp., Waltham, MA
John Duh, T. G. Matheson
Mentor Graphics Corp., Warren, NJ*

20.4S A Fast and Accurate Technique to Optimize Characterization Tables for High-Level

*John F. Croix
Advanced Micro Devices, Austin, TX
Martin D.F. Wong
Univ. of Texas, Austin, TX*



2:00
to
4:00

Session 21 Modeling and Transformations in Synthesis

Room: B7

*Chair: David Ku
Escalade Corp., Santa Clara, CA
Organizers: Kazutoshi Wakabayashi,
Raul Camposano*

Papers in this session describe innovative modeling and transformation techniques for synthesis and optimization of digital systems. The first paper describes modeling exception behaviors and its use in system level optimization. The second paper describes statistics-driven selection of transformation based on design goals. The third paper focuses on application bundling techniques in application specific programmable processor synthesis. The last paper presents new performance modeling approach for visualization and tradeoff analysis.

21.1 Limited Exception Modeling and its Use in Presynthesis Optimization

Jian Li
*Univ. of Illinois, Urbana, IL
Rajesh K. Gupta
Univ. of California, Irvine, CA*

21.2 Potential-Driven Statistics-Based Ordering of Transformations

Anna Poplawski, Toshio Misawa
*C&C Research Labs., Nec Usa, Inc., Princeton, NJ
Miodrag M. Potkonjak
Univ. of California, Los Angeles, CA*

21.3 Application Bundling During Reconfigurable Datapath Synthesis

Kyosun Kim, Ramesh Karri
*Univ. of Massachusetts, Amherst, MA
Miodrag M. Potkonjak
Univ. of California, Los Angeles, CA*

21.4 Symbolic Evaluation of Performance Models for Tradeoff Visualization

Jeffery Walrath, Ranga Vemuri
Univ. of Cincinnati, Cincinnati, OH

Session 22 Statistical Power Estimation Techniques

Room: B8

*Chair: Luca Benini
Stanford Univ., Stanford, CA
Organizers: Massoud Pedram, Andrew T. Yang*

Statistical sampling is an effective technique for accurate power evaluation across design levels. This session presents papers which apply sampling strategies to develop macromodel equations for RT-level power estimation, evaluate circuit power in sequential circuits, derive the power distribution profile in combinational circuits, and estimate the maximum instantaneous power of a circuit.

22.1 Power Macromodeling for High Level Power Estimation

Subodh Gupta, Farid N. Najm
Univ. of Illinois, Urbana, IL

22.2 Statistical Estimation of Distribution of Power Dissipation in VLSI Circuits

Chih-shun Ding, Qing Wu, Massoud Pedram -
Univ. of S. California, Los Angeles, CA

22.3 Statistical Estimation of Average Power Dissipation in Sequential Circuits

Li-Pen Yuan, Chin-Chi Teng, Sung-Mo Kang
Univ. of Illinois, Urbana, IL

22.4 Vector Generation for Maximum Instantaneous Current Through Supply Lines for CMOS Circuits

Angela Krstic, Kwang-Ting Cheng
Univ. of California, Santa Barbara, CA



Session 23 Room: A6/A7 Co-Simulation

*Chair: Kunle Olukotun
Stanford Univ., Stanford, CA
Organizers: Rajesh K. Gupta,
Kunle Olukotun*

Combined simulation of hardware and software component is key to concurrent design of embedded systems. We begin with a tutorial on latest advances in system co-simulation for DSP and control-oriented applications. The other contributions describe co-simulation as an aid to carry out system level partitioning into hardware and software, communication mechanisms to speed up simulation.

23.1 Embedded Tutorial: Advances in System-Level Co-Simulation

Joachim Kunkel
*Synopsys, Inc., Mountain View, CA
Luciano Lavagno
Cadence Berkeley Labs., Berkeley, CA*

23.2 Fast Hardware/Software Co-Simulation for Virtual Prototyping and Trade-Off Analysis

Claudio Passerone, Luciano Lavagno
*Politecnico di Torino, Torino, Italy
Massimiliano Chiodo
Alta Group, Sunnyvale, CA
Alberto Sangiovanni-Vincentelli
Univ. of California, Berkeley, CA*

23.3 Dynamic Communication Models in Embedded System Co-Simulation

Ken Hines, Gaetano Borriello
Univ. of Washington, Seattle, WA

Session 24 Room: A1 Panel: Challenges in Worldwide IP Reuse

*Chair: Rita Glover
EDA Today, Phoenix, AZ
Organizers: Takahide Inoue
Sony, Milpitas, CA
John Teets
CFI, Austin, TX
Rita Glover
EDA Today, Phoenix, AZ*

Advances in IC process technology have enabled the design of complex systems on a single chip. System-on-chip developers need to be able to mix and match predesigned best-in-class functional blocks from many providers if they are to meet design deadlines with limited design engineering resources. Consequently, there is a rising interest in interoperable blocks of intellectual property (IP). This panel explores the opportunities and challenges for design innovation offered by a worldwide, open IP reuse mechanism. The panel will begin with an embedded tutorial case study on the VSIA (Virtual Socket Interface Alliance) approach to IP reuse. Then, IP providers and users will discuss the technical and business challenges in establishing a mechanism for IP reuse. The panelists will also discuss the issues in integrating IP from multiple providers into system-on-chip designs.

24.1 Embedded Tutorial: Case Study With VSIA

Doug Fairbairn
Cadence Design Systems, Inc., San Jose, CA

Panel Members:

John Luis Boris - LSI Logic, Milpitas, CA
Doug Fairbairn - Cadence Design Systems, Inc., San Jose, CA
Takahide Inoue - Sony, Milpitas, CA
Raj Raghavan - Phoenix Tech. Ltd., Virtual Chips, San Jose, CA
Wally Rhines - Mentor Graphics Corp., Wilsonville, OR
Steve Schulz - Texas Instruments, Dallas, TX

Session 25 Room: A9/A10 Emerging Technologies and Architectures for Low Power

*Chair: Vivek Tiwari
Intel Corp., Santa Clara, CA
Organizers: Anatha Chandrakasan,
Robert C. Frye*

Tools and techniques to exploit sub-1volt technologies (low Vt and multi-Vt) are presented. Power estimation methodologies address variable voltage design and architectural transformations. Logic-level transformations for low power are evaluated in the context of a commercial microprocessor.

25.1 Device-Circuit Optimization for Minimal Energy and Power Consumption in CMOS Random Logic Networks

Pankaj Pant, Vivek De, Abhijit Chatterjee
Georgia Inst. of Tech., Atlanta, GA

25.2 A Transistor Sizing Methodology and Tool for Multi-Threshold CMOS Technology

James Kao, Anantha Chandrakasan
Massachusetts Inst. of Tech., Cambridge, MA

25.3 Architectural Exploration Using Verilog-Based power Estimation: A Case Study of the IDCT

Thucydidis Xanthopoulos, Yoshifumi Yaoi, Anantha Chandrakasan
Massachusetts Inst. of Tech., Cambridge, MA

25.4S A Power Estimation Framework for Designing Low Power Portable Video Applications

Chi-ying Tsui, Harry Chan
*Hong Kong Univ. of Science & Tech., Clear Water Bay, Hong Kong
Qing Wu, Chih-Shun Ding, Massoud Pedram
Univ. of S. California, Los Angeles, CA*

25.5S An Investigation of Power Delay Trade-Offs Using Logic and Structural Transformations: Experiments on the PowerPC

Qi Wang, Sarma Vrudhula
*Univ. of Arizona, Tucson, AZ
Shantanu Ganguly
Motorola, Austin, TX*



4:30
to
6:00

Session 26 High Level Synthesis for Low Power

Room: B7

*Chair: Kazutoshi Wakabayashi
Nec Corp., Kawasaki, Japan
Organizers: Raul Camposano, Kazutoshi
Wakabayashi*

Techniques to minimize power consumption early in the design process are gaining importance. The papers in this session include power management re-specifying the controller and configuring multiplexers, techniques based on network flow suitable for register and memory allocation, and loop folding.

26.1 Power Management Techniques for Control-Flow Intensive Designs

Anand Raghunathan, Niraj K. Jha
Princeton Univ., Princeton, NJ
Sujit Dey
C&C Research Labs., Nec Usa, Inc., Princeton, NJ
Kazutoshi Wakabayashi
NEC Corp., Kawasaki, Japan

26.2 Low Energy memory and Register Allocation Using Network Flow

Cathy Gebotys
Univ. of Waterloo, Waterloo, ON, Canada

26.3 Power-Conscious High-Level Synthesis Using Loop Folding

Daehong Kim, Kiyong Choi
Seoul National Univ., Seoul, Korea

Session 27 Module Generation

Room: B8

*Chair: Dwight D. Hill
Synopsys, Inc., Mountain View, CA
Organizers: Antun Domic, Patrick Groeneveld*

This session starts with a review of the relevant topics in module generation for submicron design. A 2-dimensional layout generator for CMOS cells and a new basis for folding algorithm will be presented. Finally, an original technology-retargeting technique is presented for CMOS cells.

27.1 Embedded Tutorial: The Future of Custom Cell Generation in Physical Synthesis

Martin Lefebvre, Said Boumaras
Cadabra Technologies, Inc., Nepean, ON, Canada
David Marple
Synopsys, Inc., Mountain View, CA

27.2S CLIP: An Optimizing Layout Generator for Two-Dimensional CMOS Cells

Avaneendra Gupta, John P. Hayes
Univ. of Michigan, Ann Arbor, MI

27.3S An Efficient Transistor Folding Algorithm for Row-Based CMOS Layout Design

Jaewon Kim
Quickturn Design Systems, Inc., Mountain View, CA
Sung-Mo Kang
Univ. of Illinois, Urbana, IL

27.4 Technology Retargeting for IC Layout

John Lakos
Mentor Graphics Corp., Warren, NJ



Session 28 Room: A6/A7 BIST and DFT

*Chair: Yervant Zorian
Logicvision, Inc., Princeton, NJ
Organizers: Janusz Rajski, Yervant Zorian*

This session presents advanced solutions in Built-In Self-Test and Design-for-Testability. The papers cover novel techniques: for partial scan flip-flop selection, for scan-based BIST with reduced random pattern resistant faults, and a greedy algorithm to select test points for BIST.

28.1 A Test Synthesis Approach to Reducing Ballast DFT Overhead

Douglas Chang, Malgorzata Marek-Sadowska, Kwang-Ting Cheng
Univ. of California, Santa Barbara, CA
Mike Tien-Chien Lee
Fujitsu Labs. of America, Inc., Santa Clara, CA
Takashi Aikyo
Fujitsu Labs., Ltd., Kawasaki, Japan

28.2 Starbist: Scan Autocorrelated Random Pattern Generation

Kun-han Tsai, Malgorzata Marek-Sadowska
Univ. of California, Santa Barbara, CA
Sybille Hellebrand
Univ. of Siegen, Siegen, Germany
Janusz Rajski
Mentor Graphics Corp., Wilsonville, OR

28.3 A Hybrid Algorithm for Test Point Selection for Scan-Based BIST

Huan-Chih Tsai, Kwang-Ting Cheng
Univ. of California, Santa Barbara, CA
Chih-Jen Lin
Intel Corp., Hillsboro, OR
Sudipta Bhawmik
Lucent Tech. Bell Labs., Princeton, NJ

Session 29 Room: A1 Panel: Hardware/Software Co-Verification

*Chair: Gary Smith
Dataquest, San Jose, CA
Organizers: Michel Courtoy
Aptix Corp., San Jose, CA
Marion Kenefick
Consultant, Los Gatos, CA*

System design issues are emerging as the top concerns of design teams today. These issues are dominated by the lack of hardware/software co-verification methodologies. Successful co-verification strategies require an environment that enables early integration of the hardware and software. The rationale of the panel is to confront ideas on how hardware/software co-verification is done for large systems. The inputs will be supplied by users and vendors supplying different solutions.

Panel Members:

Brian Bailey
Mentor Graphics Corp., Wilsonville, OR
Geoff Bunza
Eagle Design Automation/VIEWLogic, Beaverton, OR
Willis Hendley
Sun Microsystems, Inc., Chelmsford, MA
Kurt Keutzer
Synopsys, Inc., Mountain View, CA
Amr Mohsen
Aptix Corp., San Jose, CA
Richard Moseley
Motorola, Inc., Austin, TX
James Rowson
Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA

Session 30 Room: A9/A10 DSP & Telecommunication System Design

*Chair: Rajeev Jain
Univ. of California, Los Angeles, CA
Organizers: Phil Duncan, Teresa Meng*

Specific application domains often require specialized CAD tools and methodologies. This session examines unique methods of design specification, analysis and optimization within the area of DSP and telecommunication design.

30.1 Design and Synthesis of Array Structured Telecommunication Processing Applications

Wolfgang Meyer, Andrew Seawright
Synopsys, Inc., Mountain View, CA
Fumiya Tada
Hitachi Ltd., Yokohama, Japan

30.2 RASSP Virtual Prototyping of DSP Systems

Carl Hein, Junius Pridgen, Bill Kline
Lockheed Martin Advanced Tech. Labs, Camden, NJ

30.3 A Parallel/Serial Trade-Off Methodology for Look-up Table Based Decoders

Claus Schneider
Siemens AG, Munich, Germany



8:30
to
10:00

Session 31 Embedded Tutorial: High Level Power Modeling, Estimation and Optimization

Room: B7

*Chair: Massoud Pedram
Univ. of S. California, Los Angeles, CA
Organizers: Giovanni De Micheli, Massoud Pedram*

The first part of the tutorial analyzes models of power dissipation in integrated circuits, and present state-of-the-art power estimation and simulation techniques at logic level and above. The second part of the tutorial covers various design techniques for power optimization in VLSI designs.

Presenters:

Enrico Macii
Politecnico di Torino, Torino, Italy
Massoud Pedram
Univ. of S. California, Los Angeles, CA
Fabio Somenzi
Univ. of Colorado, Boulder, CO

Session 32 Advances in Partitioning

Room: B8

*Chair: Martin D.f Wong
Univ. of Texas, Austin, TX
Organizers: Antun Domic, Patrick Groeneveld*

This session presents several promising directions in system partitioning, incorporating techniques that bridge areas outside of traditional EDA. The first paper gives a new approach to hierarchy partitioning, based on a new spreading-metric concept. The second and third papers address multi-FPGA system partitioning, using HDL and netlist hierarchy as well as synthesis to achieve superior results. The fourth and fifth papers each develop promising variants of the multi-level partitioning paradigm.

32.1 A New Network Flow Approach for Hierarchical Tree Partitioning

Ming-Ter Kuo, Chung-Kuan Cheng
Univ. of California at San Diego, La Jolla, CA

32.2S Multi-Way FPGA Partitioning by Fully Exploiting Design Hierarchy

Wen-Jong Fang, Allen C.H. Wu
Tsing Hua Univ., Taiwan, ROC

32.3S A Hierarchy-Driven FPGA Partitioning Method

Helena Krupnova, Ali Abbara, Gabriele Saucier
*Inst. Nat'l Polytech de Grenoble/CSI,
Grenoble, France*

32.4S Multilevel Hypergraph Partitioning: Application in VLSI Domain

George Karypis, Rajat Aggarwal, Vipin Kumar, Shashi Shekhar
Univ. of Minnesota, Minneapolis, MN

32.5S Multilevel Circuit Partitioning

Charles J. Alpert
IBM Austin Research Lab., Austin, TX
Jen-Hsin Huang, Andrew B. Kahng
Univ. of California, Los Angeles, CA



Thursday, June 12

Session 33 Room: A6/A7 Processor Test Techniques

Chair: Janusz Rajski

Mentor Graphics Corp., Wilsonville, OR

Organizers: Yervant Zorian, Janusz Rajski

This session addresses issues in testing data path circuits in processors. The papers cover hierarchical test generation solutions for application-specific processors, frequency domain-based BIST solutions for digital filters and integrated BIST solutions for datapaths and controllers.

33.1 Hierarchical Test Generation and Design for Testability of ASPPs and ASIPs

Indradeep Ghosh, Anand Raghunathan, Niraj K. Jha

Princeton Univ., Princeton, NJ

33.2 Frequency-Domain Compatibility in Digital Filter BIST

Laurence Goodby, Alex Orailoglu

Univ. of California, La Jolla, CA

33.3 A Scheme for Integrated Controller-Datapath Fault Testing

Mehrdad Nourani, Joan E. Carletta,

Christos Papachristou

Case Western Reserve Univ., Cleveland, OH

Session 34 Room: A1 Panel: The Next Generation HDL

Chair: Steven E. Schulz

Texas Instruments, Dallas, TX

Organizers: Richard Goering

EE Times, Felton CA

Nanette Collins

Consultant, Boston, MA

The recent market battle between VHDL and Verilog HDL has obscured the larger issue of whether either of these languages is adequate for next-generation design. Can they be extended, or do we need an entirely new language that constructed to handle system-level design descriptions, behavioral and logic synthesis, simulation, and formal verification? If so, how should that language be created? Panelists will present differing views on this subject. The panel, comprised of designers, noted university professors and EDA manufacturers, is geared toward the electronics designer.

Panel Members:

Gerard Berry

Ecole des Mines de Paris, Sophia-Antipolis, France

Kurt Keutzer

Synopsys, Inc., Mountain View, CA

Maq Mannan

National Semiconductor Corp., Santa Clara, CA

James A. Rowson

Alta Group of Cadence Design Systems, Inc, Sunnyvale, CA

Alberto Sangiovanni-Vincentelli
Univ. of California, Berkeley, CA

Larry Saunders

SEVA Technologies, San Diego, CA

*"This Panel is Co-Organized by
IEEE Design & Test of Computers
Magazine"*

Session 35 Room: A9/A10 Design Processes and Frameworks

Chair: Teresa Meng

Stanford Univ., Stanford, CA

Organizers: Teresa Meng, Jan M. Rabaey

Design is a multi-domain problem possibly separated over a geographic distance. To achieve effective design, one must integrate design teams locally and across corporate borders. In addition, the timely availability of information on components and designs throughout the design team is a requirement. This session looks at distributing collaborative design and component information across the internet, along with frameworks to tie tools together at a site.

35.1 Executable Workflows: A Paradigm for Collaborative Design on the Internet

Hemang Lavana, Amit Khetawat, Franc Brglez

N. Carolina State Univ., Raleigh, NC

Krzysztof Kozminski

National Semiconductor Corp., Santa Clara, CA

35.2 Electronic Component Information Exchange (ECIX)

Donald Cottrell, Sarah Logsdon

CFI, Inc., Austin, TX

35.3 Modeling Design Tasks and Tools - The Link Between Product and Flow Model

Bernd Schürmann, Joachim Altmeyer

Univ. of Kaiserslautern, Kaiserslautern, Germany



10:30
to
12:00

Session 36

Probabilistic Models of Input Data for Efficient Power Estimation

Room: B7

*Chair: Farid N. Najm
Univ. of Illinois, Urbana, IL
Organizers: Fabio Somenzi, Andrew T. Yang*

Dynamic power estimation can be significantly sped up by probabilistic modeling of input sequences. The resulting models can then be used to compact the initial sequence or to develop hybrid multi-level power estimation techniques. Papers in this session describe application of such probabilistic modeling techniques in various contexts.

36.1 Power Estimation Using Hierarchical Markov Models

Radu Marculescu, Diana Marculescu,
Massoud Pedram
Univ. of S. California, Los Angeles, CA

36.2 Profile-Driven Program Synthesis for Evaluation of System Power Dissipation

Cheng-ta Hsieh, Massoud Pedram
Univ. of S. California, Los Angeles, CA

36.3 Analytical Estimation of Transition Activity From Word-Level Signal Statistics

Sumant Ramprasad, Naresh R. Shanbhag,
Ibrahim N. Hajj
Univ. of Illinois, Urbana, IL

Session 37

Hot Topics in Routing

Room: B8

*Chair: Carl Sechen
Univ. of Washington, Seattle, WA
Organizers: Patrick Groeneveld, Antun Domic*

This session addresses relevant topics for routing in deep submicron IC's. New results in wire sizing and wire segmenting for optimum speed will be presented in two papers. A fresh look at multi layer assignment will be presented, as well as a solid practical approach to clock routing.

37.1 Wire Segmenting for Improved Buffer Insertion

Charles J. Alpert, Anirudh Devgan
IBM Austin Research Lab., Austin, TX

37.2 Practical Bounded-Skew Clock Routing

Andrew B. Kahng, C.-W. Albert
Univ. of California, Los Angeles, CA

37.3S An Efficient Approach to Multi-Layer Layer Assignment with applications to VIA Minimization

Chin-Chih Chang, Jason Cong
Univ. of California, Los Angeles, CA

37.4S Optimal Wire-Sizing Function with Fringing Capacitance Consideration

C.P. Chen, D.F. Wong
Univ. of Texas, Austin, TX

Session 38 Room: A6/A7 Test Generation and Fault Simulation

*Chair: Vishwani Agrawal
Lucent Tech. Bell Labs., Murray Hill, NJ
Organizers: Yervant Zorian, Janusz Rajski*

This session covers advancements in fault simulation and test generation. The papers cover improved fault simulation procedures based on multiple observation time, optimized automatic test pattern generation for power dissipation, and advanced test pattern generation for asynchronous control circuits.

38.1 Fault Simulation Under the Multiple Observation Time Approach Using Backward Implications

*Irith Pomeranz, Sudhakar M. Reddy
Univ. of Iowa, Iowa City, IA*

38.2 ATPG for Heat Dissipation Minimization for Scan Testing

*Seongmoon Wang, Sandeep K. Gupta
Univ. of S. California, Los Angeles, CA*

38.3 Automatic Generation of Synchronous Test Patterns for Asynchronous Circuits

*Oriol Roig, Jordi Cortadella, Marco A. Peña, Enric Pastor
Univ. Politècnica de Catalunya, Barcelona, Spain*

Session 39 Room: A1 Panel: The Road Ahead in CPLD & FPGA Design Methodology

*Chair: Rhondalee Rohleder
Pace Technologies, Scottsdale, AZ
Organizer: John Birkner
QuickLogic Corp., Sunnyvale, CA*

This panel of industry experts will explore the opportunities and challenges of designing with large capacity CPLDs and FPGAs. As densities grow beyond 20,000 gates, there is a disconnect between the cutting-edge EDA tools featured in trade shows and the more ordinary tools used by the typical programmable logic designer as s/he moves to a higher level design methodology. a three-to-five year roadmap will guide this discussion of the future of synthesis and simulation, the impact of HDLs on complex devices, and the role of intellectual property and universal tools in the CPLD & FPGA design scape.

Panel Members:

*Robert K. Beachler
Altera Corp., San Jose, CA
Mike Dini
The Dini Group, La Jolla, CA
Bob Donaldson
Annapolis Micro Systems, Inc., Annapolis, MD
Don Faria
Synopsys, Inc., Mountain View, CA
Steve Golson
Trilobyte Systems, Carlisle, MA
Bruce Kleinman
QuickLogic Corp., Sunnyvale, CA
Dave Kohlmeier
Synario Design Automation, Redmond, WA
Rhondalee Rohleder
PACE Technologies, Scottsdale, AZ*

Session 40 Room: A9/A10 Deep Submicron Modeling and Analysis

*Chair: Robert C. Frye
Lucent Tech. Bell Labs., Murray Hill, NJ
Organizers: Vivek Tiwari, Anantha Chandrakasan*

Deep sub-micron design brings with it a host of problems in terms of modeling and analysis. This session addresses issues such as capacitance extraction methodologies, noise analysis and sub-micron timing models.

40.1 Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology

*Jason Cong, Lei He, Andrew B. Kahng
Univ. of California, Los Angeles, CA
David Noice, Nagesh Shirali,
H.C. Steven Yen
Cadence Design Systems, Inc., San Jose, CA*

40.2 Accurate and Efficient Timing Models of Submicron Digital Standard Cells

*Cristiano Forzan, Bruno Franzini, Carlo Guardiani
SGS-Thomson Microelectronics, Agrate Brianza, Italy
Sungsoo Hong
Seoul National Univ., Seoul, Korea*

40.3 Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design

*Howard H. Chen, David D. Ling
IBM Corp., Yorktown Heights, NY*



Thursday, June 12

2:00
to
4:00

Session 41 Technology-Dependent Optimization for Performance and Power

Room: B7

*Chair: Gabriele Saucier
Inst. Nat'l Polytech de Grenoble/csi, Grenoble,
France
Organizers: Jason Cong, Gabriele Saucier*

This session is devoted to technology-dependent performance and power optimization. It includes technology mapping with retiming and pipelining for FPGAs, layout-driven logic transformation, and post-layout optimization for ASICs.

41.1 Performance-Driven FPGA Synthesis with Retiming and Pipelining for Sequential Circuits

Jason Cong, Chang Wu
Univ. of California, Los Angeles, CA

41.2 Technology-Dependent Transformations for Low-Power Synthesis

Rajendran V. Panda
Motorola, Inc., Austin, TX
Farid N. Najm
Univ. of Illinois, Urbana, IL

41.3 Low Power FPGA Design - A Reengineering Approach

Chau-Shen Chen, Ting Ting Hwang
Tsing Hua Univ., Taiwan, ROC
C.L. Liu
Univ. of Illinois, Urbana, IL

41.4S Post-Layout Logic Restructuring for Performance Optimization

Yi-Min Jiang, Angela Krstic, Kwang-Ting Cheng,
Malgorzata Marek-Sadowska
Univ. of California, Santa Barbara, CA

41.5S Layout Driven Re-Synthesis for Low Power Consumption LSIs

Masako Murofushi, Takashi Ishioka, Masami
Murakata, Takashi Mitsuhashi
Toshiba Corp., Kawasaki, Japan

Session 42 CAD Issues for Micro-Electro-Mechanical Systems

Room: B8

*Chair: Randolph E. Harr
DARPA/ETO, Arlington, VA
Organizers: Randolph E. Harr, Jacob White*

The use of micro-electro-mechanical systems (MEMS) integrated with electronics is appearing in a wide range of systems such as in pressure sensors, air-bag accelerometers and ink-jet printheads. This diversity of applications require new and innovative CAD tools to enable the design of this new mixed technology. This session begins with overviews of MEMS technology and design, pointing out the CAD issues, and then features some early simulation and synthesis tool developments.

42.1 Embedded Tutorial: Overview of Microelectromechanical Systems and Design Processes

William Tang
Jet Propulsion Lab., Pasadena, CA

42.2 CAD and Foundries for Microsystems

Jean-michel Karam, Bernard Courtois, H. Boutamine
TIMA Lab., Grenoble, France
P. Drake

Mentor Graphics Corp., Berkshire, UK

A. Poppe, V. Szekely, M. Rencz
Technical Univ. of Budapest, Budapest, Hungary

K. Hofmann, Manfred Glesner
Darmstadt Univ. of Tech., Darmstadt, Germany

42.3 Structured Design of Microelectromechanical Systems

Tamal Mukherjee, Gary K. Fedder
Carnegie Mellon Univ., Pittsburgh, PA

42.4 Algorithms for Coupled Domain MEMS Simulation

N. R. Aluru, Jacob K. White
Massachusetts Inst. of Tech., Cambridge, MA



Session 43 Room: A6/A7 Hardware/Software Partitioning

*Chair: Rolf Ernst
Tech. Univ. Braunschweig, Braunschweig,
Germany
Organizers: Luciano Lavagno, Rajesh K. Gupta*

Hardware/software partitioning strongly affects the quality of overall system designs. Papers in this session address this problem under various cost/performance metrics. The first paper examines structural partitioning. The second paper considers power as a part of the cost function. The partitioning, scheduling and allocation tasks are strongly inter-related as pointed out in the remaining papers.

43.1 A Hardware/Software Partitioner Using a Dynamically Determined Granularity

Joerg Henkel
*NEC USA, Inc., Princeton, NJ
Rolf Ernst
Tech. Univ. Braunschweig, Braunschweig,
Germany*

43.2 System-Level Synthesis of Low-Power Hard Real-Time Systems

Darko Kirovski, Miodrag M. Potkonjak
Univ. of California, Los Angeles, CA

43.3 COSYN: Hardware-Software Co-Synthesis of Embedded Systems

Bharat P. Dave, Ganesh Lakshminarayana, Niraj K. Jha
Princeton Univ., Princeton, NJ

43.4S Data-Flow Assisted Behavioral Partitioning for Embedded Systems

Samir Agrawal
*Synopsys, Inc., Mountain View, CA
Rajesh K. Gupta
Univ. of California, Irvine, CA*

43.5S Hardware/Software Partitioning and Pipelining

Smita Bakshi, Daniel D. Gajski
Univ. of California, Irvine, CA

Session 44 Room: A1 Panel: Noise and Signal Integrity in Deep Submicron Design

*Chair: William E. Guthrie
Collett International, Inc., Santa Clara, CA
Organizer: Massoud Pedram*

Sub-half-micron process technologies are creating a fundamental shift in the problems faced by IC designers and fabricators. As geometries shrink, signal integrity and noise play a critical role in determining IC performance. Without accurate interconnect data and detailed noise analysis tools, designers cannot assess the quality of their designs and/or new processes. This panel will offer designers an opportunity to understand the complex analysis and design issues that surround the noise and signal integrity problem. In particular, it will discuss conditions under which designers face serious noise and signal integrity problems, summarize state-of-the-art in methodologies and tools for interconnect extraction and signal integrity analysis, and present design techniques and CAD tools for noise avoidance. Finally, design challenges and tool requirements for noise analysis and management in next-generation ICs will be debated.

44.1 Embedded Tutorial: Chip Parasitic Extraction and Signal Integrity Verification

Wayne Dai
Univ. of California, Santa Cruz, CA

Panel Members:

Rakesh Chadha
Bell Labs. Design Automation, Murray Hill, NJ
Jason Cong
Univ. of California, Los Angeles, CA
Anirudh Devgan
IBM Austin Research Lab., Austin, TX
Charlie Huang
EPIC Design Technology Inc., Sunnyvale, CA
Tom J. Mozden
Intel Corp., Chandler, AZ
Andrew T. Yang
Avant! Corp., Sunnyvale, CA

Session 45 Room: A9/A10 Designing High Performance and Low Power Microprocessors Using Full Custom Techniques

*Chair: Anantha Chandrakasan
Massachusetts Inst. of Tech., Cambridge, MA
Organizer: Anantha Chandrakasan*

This session will describe the full custom design methodology and supporting CAD technologies used to develop ALPHA and StrongARM microprocessors. The overview of the methodology will lead into three additional design related areas: low-power, electrical verification, and timing verification.

45.1 Full-Custom CMOS Design Methodology at Digital Equipment Corp.

William J. Grundmann
Digital Equipment Corp., Hudson, MA

45.2 Design of High Performance Low Power Microprocessor

Dan Dobberpuhl
Digital Equipment Corp., Hudson, MA

45.3 Full-Custom Design Benefits and Verification Headaches

Randy L. Allmon
Digital Equipment Corp., Hudson, MA

45.4 Racing Against Time: Full Custom Timing Verification

Nicholas L. Rethman
Digital Equipment Corp., Hudson, MA



4:30
to
6:00

Session 46 Formal Verification Techniques

Room: B7

*Chair: Rich Goldman
Synopsys, Inc., Mountain View, CA
Organizers: Andreas Kuehlmann, Fabio Somenzi*

This session explores three approaches to the verification of large systems. The first paper addresses the problem of reachability analysis with BDDs. The second paper combines structural and functional analysis in the verification of assertions for which either technique alone is inadequate. The last paper explores the use of tours covering all the transitions of a reduced model as a way to bridge the gap between formal methods and simulation.

46.1 Disjunctive Partitioning and Partial Iterative Squaring: An Effective Approach for Symbolic Traversal of Large Circuits

Gianpiero Cabodi
Politecnico di Torino, Torino, Italy
Paolo E. Camurati
Univ. Di Udine, Torino, Italy
Luciano Lavagno, Stefano Quer
Politecnico Di Torino, Torino, Italy

46.2 An Efficient Assertion Checker for Combinational Properties

Gagan Hasteer
Univ. of Illinois, Urbana, IL
Anmol Mathur
Silicon Graphics Corp., Mountain View, CA
Prithviraj Banerjee
Northwestern Univ., Evanston, IL

46.3 Toward Formalizing a Hybrid Verification Methodology

Aarti Gupta, Pranav Ashar
C&C Research Labs., NEC USA, Inc., Princeton, NJ
Sharad Malik
Princeton Univ., Princeton, NJ

Session 47 Placement Techniques

Room: B8

*Chair: Malgorzata Marek-sadowska
Univ. of California, Santa Barbara, CA
Organizers: Patrick Groeneveld, Antun Domic*

The session opens with an overview of a leading-edge quadratic placement system. The next paper raises intriguing questions about the advantages and implementation of the quadratic placement technique. The third paper addresses the important question of constraint budgeting and its effect on the difficulty of timing-driven placement. The final paper integrates several distinct methods to develop a new block placement approach.

47.1 Algorithms for Large-Scale Flat Placement

Jens Vygen
Univ. of Bonn, Bonn, Germany

47.2 Quadratic Placement Revisited

Charles J. Alpert
IBM Austin Research Lab., Austin, TX
Tony F. Chan, Dennis J.H. Huang, Igor L. Markov, Kenneth Y. Yan
Univ. of California, Los Angeles, CA

47.3S Unification of Budgeting and Placement

Majid Sarrafzadeh, David Knol
Northwestern Univ., Evanston, IL
Gustavo Tellez
IBM Corp., Yorktown Heights, NY

47.4S Cluster Refinement for Block Placement

Jin Xu, Pei-ning Guo, Chung-Kuan Cheng
Univ. of California at San Diego, La Jolla, CA



Session 48 Room: A1

Panel: The EDA Startup Experience: Financing the Venture

Chair: A.k. Kalekos

Telos Venture Partners, Santa Clara, CA

Organizers: Mike Murray

Acuson Corp., Mountain View, CA *A.K.*

Kalekos

Telos Venture Partners, Santa Clara, CA

Over 90% of EDA companies have been venture capital funded. What has been the relationship between entrepreneurs and venture capitalists over the years, and how is it going to evolve in the future? Is the EDA industry consolidation affecting investment opportunities in new start ups? What are VC's looking for? How can you get funding for a new company? What are the alternatives to VC funding? Get the answers to these questions from successful EDA company founders, CEOs, and venture capitalists.

Panel Members:

John Cooper

Cooper and Chyan Technology, Inc., Cupertino, CA

Penny Herscher

Simplex Solutions, Inc., San Jose, CA

Peter O'dryna

Precedence, Inc., Campbell, CA

Marty Walker

Frequency Technology, Inc., Los Altos, CA

Venture Capitalist 1 - TBD

Venture Capitalist 2 - TBD

(No badge required to attend this session)

Session 49 Room: A9/A10 Heterogeneous System Analysis

Chairs: Randolph E. Harr

DARPA/ETO, Arlington, VA

Richard Smith

Cadence Design Systems, Inc., Irving, TX

Organizers: David Blaauw, Jan M. Rabaey

Complex system design integrates a variety of heterogeneous components with varying demands regarding modeling, simulation and verification. A number of different aspects of heterogeneous system design are highlighted in this session, including hardware/software co-simulation, modeling of opto-electronic systems and audio processors.

49.1 Computer-Aided Design of Free-Space Opto-Electronic Systems

S.P. Levitan

Univ. of Pittsburgh, Pittsburgh, PA

P.J. Marchand

Univ. of California, La Jolla, CA

T.P. Kurzweg, M.A. Rempel, D.M. Chiarulli *Univ. of Pittsburgh, Pittsburgh, PA*

C. Fan, F.B. McCormick

Univ. of California, La Jolla, CA

49.2 Hardware/Software Co-Simulation in a VHDL-Based Test Bench Approach

Wolfgang Ecker, Matthias Bauer

Siemens Ag, Munich, Germany

49.3 An Embedded System Case Study: The Firmware Development Environment for a Multimedia Audio Processor

Clifford Liem, Ahmed A. Jerraya

Inst. Nat'l Polytech de Grenoble/CSI, Grenoble, France

Marco Cornero, Miguel Santana, Pierre Paulin
SGS-Thomson, Grenoble, France

Jean-Marc Gentit, Jean Lopez, Xavier Figari, Laurent Bergher

Thomson Consumer Electronic Comp., Meylan, France



Friday, June 13

34th dac Full Day Tutorials

Tutorials will be held at the Anaheim Convention Center

8:00 AM - Tutorial Registration Opens

12:00 Noon - Lunch

8:30 AM - Continental Breakfast

5:00 PM - Tutorials End

9:00 AM - Tutorials Begin

Tutorial One

asic delay calculation and dcl

Organizer: Jay Abraham - CFI, Inc., Austin, TX

Presenters: Jay Abraham - CFI Inc., Austin TX Steve Mecham - Symbios Logic, Fort Collins, CO

Audience: The intended audience for this tutorial are; ASIC Library developers, EDA application developer and EDA system integrators.

Description: As ICs are crossing the .5 μ m barrier, the complexity of accurately characterizing designs in a manner that allows for efficient EDA processing has become a major technological challenge. Of particular importance are the effects of both device and interconnect properties on the overall timing of signals as they traverse paths in the design. In such designs, interconnect delays tend to dominate over cell delays. The Delay Calculation Language (DCL) Standard has been brought about to address the challenges of TIMING and POWER calculation for deep submicron designs. This tutorial will introduce the audience to the ASIC Delay Calculation Standardization effort being undertaken by IEEE and a large number of industry companies worldwide. An in-depth functional description of the DCL language and the associated EDA application Programming Interface (DCL-PI) will be presented. Specific emphasis will be placed on implementing ASIC libraries in DCL and writing EDA applications that work with DCL. Real world examples of libraries written in DCL and applications extracting delay and power information from compiled DCL libraries will be presented.

Tutorial Two

reconfigurable systems: logic emulation, custom computing, and beyond

Organizer: Scott Hauck - Northwestern Univ., Evanston, IL

Presenters: Michael Butts - Quickturn Design Systems, Inc., Portland, OR James Gateley - Sun Microsystems, Inc., Mountain View, CA Scott Hauck - Northwestern Univ., Evanston, IL Brad Hutchings Brigham Young Univ., Provo, UT Mark Shand - Digital Equipment Corp., Palo Alto, CA

Audience: This tutorial is intended for CAD and hardware researchers, digital logic designers, and others interested in the new opportunities presented by FPGAs. Only a basic knowledge of CAD tools and digital logic design is required.

Description: Field-Programmable Gate Arrays (FPGAs) are chips that can be electrically programmed and reprogrammed to implement complex, multi-level logic. While commonly thought of as an implementation medium for glue-logic on circuit boards, they offer great potential for many roles. As a logic emulation system, they offer orders of magnitude speedup for the simulation and verification of integrated circuits. As a custom-computing device, they provide world-class performance for numerous applications. In this tutorial we will discuss these new opportunities enabled by FPGA technology, focusing both on what is now possible with current technology, as well as presenting critical areas for further innovation. Scott Hauck will begin the presentation by reviewing FPGA technology, highlighting their unique features. He will also explain how these chips enable new applications, including multi-mode, logic emulation, custom-computing, and run-time

Tutorial
Two
cont.

reconfiguration systems. Michael Butts will then focus on how FPGAs have revolutionized logic validation. By considering current and future logic emulation and rapid-prototyping hardware. He will explain how these systems provide huge speedups for functional simulation. Brad Hutchings will cover the use of FPGAs for custom computing machines, systems which provide extremely fast implementations for many different applications. He will also discuss run-time reconfiguration, a promising new technology for multi-tasking digital hardware which may be key to future high-performance computing. Although much of FPGA-based system work has been driven by chip technology, software support for these systems is just as critical as efficient hardware. Scott Hauck will present both the successes and remaining challenges of current CAD tools for multi-FPGA systems. We will conclude the presentation by focusing on user experiences with FPGA-based systems. James Gateley of Sun Microsystems will explain how logic emulation systems have helped validate several of Sun's advanced microprocessors.

Then Mark Shand, part of Digital Equipment Corporation's seminal DecPerLe project, will discuss how FPGA technology has enabled his group to produce world-class performance, at a relatively low cost, for a huge set of applications. We will also feature demonstrations of current commercial and research reconfigurable systems. This will provide attendees a chance to explore this powerful new computing paradigm.

system-design using ic cores:design, test and sign-off

Organizer: Rajesh K. Gupta - Univ. of California, Irvine, CA

Presenters: Rajesh K. Gupta - Univ. of California, Irvine, CA Ramsey Haddad - Synopsys, Inc., Mountain View, CA Rob Roy - NEC, Princeton, NJ

Audience: This tutorial is targeted for engineers who are either building core cells or using cores in their system design. CAD developers and researchers will develop an appreciation of the design tool requirements and sign-off issues in using cores.

Description: Core-based designs are becoming common due to increased complexity of systems and a drive to reuse previous design efforts. Core-based designs represent a special challenge in almost all aspects of IC/System design because of the requirements to integrate diverse components with little or no modifications to individual block or core cells. Tools and methodologies are needed for design and validation. In this tutorial we present the current status in availability and usability of core cells. The presentation is roughly divided into three parts: (a) IC design and synthesis techniques for cores, do's and don'ts based on case studies, available standards that the core builders and users can adhere to; (b) system validation using co-simulation tools; (c) access mechanisms and testability aspects in making cores and core-based designs easily testable and diagnosable using structured DFT and BIST approaches.

We address issues that a core user faces in selecting and successfully incorporating reusable core cells in his or her product designs. We will examine hard, firm and soft cores. In each case, what are the challenges of integrating the reusable components? Whose problems are they? Yours or your core supplier? Finally, we discuss the issue of interface abstraction for core cells in the context of its reusability, i.e., what interface(s) should a designer target for maximum reusability? We present current and potential future (bus) standards in interfacing cores.

The presentation will include pointers to resources on currently available cores, IP providers and design tools. We will examine the progress and future progress in on-going standardization efforts such as the industry-wide Virtual Sockets initiative.

Tutorial
Three



interconnect-driven performance optimization for deep submicron layout systems

Organizer: Jason Cong - Univ. of California, Los Angeles, CA

Presenters: David Blaauw - Motorola, Inc., Austin, TX, Jason Cong - Univ. of California, Los Angeles, CA, Ren-Song Tsay - Axis Systems, Santa Clara, CA

Audience: This tutorial is intended for the researchers and practitioners who are interested in research and development of the new generation of VLSI layout systems for deep submicron design. Basic knowledge of VLSI CAD, especially physical design, would be helpful.

Description: This tutorial presents state-of-art timing models, design methodology, and optimization techniques for performance optimization in deep submicron layout. Much emphasis will be given on modeling and optimization of interconnects, which have become the determining factor of circuit performance. The tutorial includes the following components:

(1) Timing models: We shall present various interconnect and device models of different degrees of accuracy and efficiency for layout optimization in deep submicron designs, including simple lumped RC models, high-order interconnect models using moment matching, accurate device models with consideration of input waveform and interconnect resistance shielding in deep submicron design.

(2) Performance-driven layout methodology: We shall discuss how performance issues can be managed with appropriate methodology throughout the entire design process, how physical design tools interact with high-level/logical-level synthesis tools and how various layout optimization techniques can impact design performance. We shall also review and analyze current design flow provided by commercial CAD vendors.

(3) Performance optimization techniques in layout: We shall present a wide range of layout design and optimization techniques for performance-driven floorplanning, placement, global and detailed routing. We shall emphasize recent advances on timing budgeting, timing-driven placement, interconnect topology optimization with buffer insertion, optimal wiresizing, simultaneous device and wiresizing, and layout optimization of high-speed clocks.

(4) Industrial Application of High Performance Layout Methods: We will present an in-depth analysis of how the different modeling and optimization techniques are applied in an industrial setting. Practical constraints and limitations in the area of clock skew minimization, device delay modeling and optimization, noise analysis and mitigation, and power and ground routing and analysis will be covered. We will emphasize overall design flow approaches and issues, high performance design considerations, and data from actual design case studies.

David Blaauw, Motorola, Austin, TX, is managing the High Performance Design Technologies group. His work is aimed at technologies for analysis and optimization of high performance design.

Jason Cong, Univ. of California, Los Angeles, Ca, is an Associate Professor and Co-Director of VLSI CAD Laboratory in the Computer Science Department, where he is leading the research on performance-driven highly-scalable layout systems for next generation of VLSI systems.

Ren-Song Tsay, Axis Systems, Santa Clara, CA, was Chief Architect and Director of Product Management and Technology Programs at Avant! Corp. from 1992 to 1996. Since 1997, he is a co-founder and VP of Software Systems of Axis Systems.



Tutorial Five

asic delay and power calculation

Organizer: Jay Abraham - CFI, Inc., Austin, TX

Presenters: Jay Abraham - CFI Inc., Austin, TX, Steve Mecham - Symbios Logic, Fort Collins, CO, Karla Reynolds - IBM Microelectronics., Essex Junction, VT

Audience: The intended audience for this tutorial includes: ASIC Library developers, EDA application developers and EDA system integrators.

Description: As ICs are crossing the 0.5um barrier, the complexity of accurately characterizing designs in a manner that allows for efficient EDA processing has become a major technological challenge. In such designs, interconnect delays tend to dominate over cell delays. Low power designs require accurate power modeling. The Delay Calculation language (DCL) Standard has been brought about to address the challenges of TIMING and POWER calculation for deep submicron designs.

This tutorial will introduce the audience to the ASIC Delay Calculation Standardization effort being undertaken by IEEE and a large number of industry companies world-wide. An in-depth functional description of the DCL language and the associated EDA application Procedural Interface (DCL-PI) will be presented. Specific emphasis will be placed on implementing ASIC libraries in DCL and writing EDA applications that work with DCL. The Standard Parasitics Exchange Format (SPEF) and Physical Design Exchange Format (PDEF) will also be presented. Real-world examples of libraries written in DCL and applications extracting delay and power information from compiled DCL libraries will be shown.

Tutorial Six

introduction to java™ programming

Organizers: Jean Brouwers - Sun Microsystems, Mountain View, CA
Patricia Meyer-Sun Microsystems, Mountain View, CA, David Plotkin - Sun Microsystems, New York, NY

Presenters: Morgan Herrington - Sun Microsystems, Beaverton, OR, David Plotkin - Sun Microsystems, New York, NY

Audience: This tutorial is intended for software developers who are interested in a first introduction to Java™ as a programming language. Familiarity with object oriented programming languages like C/C++ is a prerequisite for this tutorial.

Description: Java™, the new programming language from SUN, has been gaining much attention. although commonly thought of as a way to add contents to Web pages and as a "better C++" programming language, it has evolved into much more. Java™ is becoming known as a computing platform — the base for all new software development and deployment. With Java™, developers can build a wide variety of applications, from traditional office automation tools like spread sheets and word processors to mission-critical client-server applications for business users and design tools used in engineering environments. Java™ can be used to implement entirely new applications or as an extension language or a front-end for an existing application. Applications written in Java™ are extremely portable and run as applets embedded in a Web browser or as multi-tiered applications distributed across the Inter-/Intranet.

This tutorial offers an introduction to the Java™ programming language.

Topics to be covered include the Java™ language, the basic Java™ development environment, Java™ run-time environments, Java™ classes and examples. The examples will be available on the Web for downloading immediately after the tutorial.



Friday, June 13

Tutorial Seven

advanced java™ topics

Organizers: Jean Brouwers - Sun Microsystems, Mountain View, CA, Patricia Meyer - Sun Microsystems, Mountain View, CA

Presenters: TBD

Audience: This tutorial is intended for software developers, system architects or product designers considering developing new products in Java™. Some familiarity with the Java™ programming language and the development and run-time environments for Java™ is required.

Description: Major corporations are developing and depolying Java™-based applications which combine the advantages of network computing with the economics of centralized computing. The main benefits of Java™-based computing include faster development, simplified administration and increased security especially improved scalability and better extensibility. Typically, business-critical applications are based on two- or three-tier client-server architectures distributed across the intra- and internet. In contrast, current EDA applications are often large, monolithic tool suites running on high performance desktop machines. Future EDA tools will move towards a multi-tiered and client-server paradigm in order to take better advantage of the available resources on the network and to cope more effectively with continuously increasing design complexity.

This tutorial will address several of the larger issues involved in developing web-centric applications based on Java™. The topics to be covered include:

- 1) Multi-tiered, web-based application architectures
- 2) Visual components, classes and tools for Java™
- 3) Interfaces of Java™ and legacy code
- 4) Java™ security

Each topic will be presented by a different speaker from the industry.