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Management Day at 42nd Design Automation Conference Focuses on Intersection of Business and Technology

BOULDER, Colo. □ May 2, 2005 □ The Design Automation Conference (DAC), the electronic design automation (EDA) industry's premier event, will offer a Management Day track on Tuesday, June 14, 2005 designed to provide managers with timely information to help them make decisions where business and technology intersect.

“Management Day @ DAC” is organized by Yervant Zorian, Virage Logic and Ahmed Jerraya, TIMA Lab and the Europe/Middle Eastern Representative to the DAC Executive Committee. The day's events will include a CEO panel and two afternoon sessions featuring presentations by managers representing the entire community of EDA tool users, including systems companies, fabless companies and independent device manufacturers (IDMs) and access to the 10th Annual EDA Business Forum luncheon.

“This innovative track provides a unique opportunity for managers to gain insights from their peers in the industry. The Management Day organizers have selected a slate of timely, informative and practical presentations designed to aid managers in decision making and problem solving,” said Bill Joyner, general chair of the 42nd DAC.

The CEO panel, moderated by Jay Vleeschhouwer of Merrill Lynch, will feature CEOs of the three major EDA vendors – Michael J. Fister, CEO, Cadence Design Systems; Walden Rhines, CEO, Mentor Graphics; and Aart De Geus, CEO, Synopsys – along with peers from IP and manufacturing; Warren East, CEO, ARM Ltd. and Jackson Hu, CEO,

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UMC, discussing the initial planning phase of bringing a new product to market and challenges of working together with partner companies to maximize success.

The first afternoon session, chaired by Dennis C. Wassung, Jr. of Adams Harkness, will provide insights on choosing EDA flows and methodologies for SoC design. Speaker Magdy Abadir of Freescale Semiconductor will discuss “EDA Flows: Best-of-Breed versus Single-Vendor Solution?” Mark Bapst, also of Freescale Semiconductor, will present criteria for selecting between an ASIC and a foundry model. Norbert Diesing and Colin Harris of PMC-Sierra will provide an overview of how to choose from all the process nodes, IP cores, and other SoC suppliers.

A second afternoon session chaired by Nic Mokhoff of EE Times will provide information to help managers determine the necessity for emerging solutions.

Kamalesh N. Ruparel, Cisco Systems, will present, “Yield is all that Matters: How do you Judge Return on Investment?” Hao Nham, eSilicon, will discuss how to meet time-to-volume requirements. Kee Sup Kim, Intel Corp. will offer “Soft Errors: Do You Need to Worry, and When? Which Applications are Affected?” Francesco Pessolano of Philips Semiconductors will discuss how to make decisions on low-power design.

The registration fee for Management Day @ DAC is \$75 and includes the luncheon and evening cocktail reception. To register for the track, visit the DAC Web site:

www.dac.com.

About DAC

DAC is the annual event where the electronics design community meets for a week-long forum of information exchange on management practices, products, methodologies and processes. Attended by more than 10,500 developers, designers, researchers, managers and

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engineers from leading electronics companies and universities worldwide, it offers a robust technical program covering the industry's hottest trends. Its vibrant exhibit floor includes more than 225 companies, many of whom are startups just introducing their first products. The conference is sponsored by the Association for Computing Machinery's Special Interest Group on Design Automation (ACM/SIGDA), the Circuits and Systems Society and Computer Aided Network Design Technical Committee of the Institute of Electrical and Electronics Engineers (IEEE/CASS/CANDE) and the Electronic Design Automation Consortium (EDA Consortium). More details about DAC are found at: www.dac.com.

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