



**FOR IMMEDIATE RELEASE**

**News Release**

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**44th Design Automation Conference to Feature Two Workshops Addressing Low Power**

*Attendees Can Learn about Proposed Standards in In-Depth, Interactive Sessions*

**BOULDER, Colo.** — April 24, 2007 — The 44th Design Automation Conference (DAC), to be held at the San Diego Convention Center, San Diego, Calif., June 4 – 8, 2007, will offer two workshops on low power design on Sunday, June 3. The *Low Power Coalition (LPC) Workshop - Standards for Low Power Design Intent*, to be held Sunday from 12:30 - 3:30 p.m., will present the benefits of using the Common Power Format (CPF) specification to capture and communicate low power constraints throughout the IC design flow. This workshop also will cover some of the recent activity and planned roadmap of the LPC. Later that day, from 4:00 - 7:00 p.m., the *Design and Verification of Low Power ICs* workshop will be held, providing information for engineers and tool developers on the Unified Power Format (UPF), including its purpose, technical constructs and usage. Leading EDA suppliers also will illustrate UPF interoperability in a multi-vendor flow.

“DAC provides the industry with tremendous opportunities for exchanging information on current design challenges and emerging issues,” said Steve Levitan, general chair of the 44th annual DAC. “The fact that there are two workshops on low power design at DAC this year underscores the importance of the topic and the value of attending DAC to get details on all of the latest developments in design.”

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**Workshop Agenda: Low Power Coalition Workshop - Standards for Low Power Design Intent  
Sunday, June 3, 2007, 12:30 - 3:30 p.m. | Room: 6D**

- I. Introduction to the Low Power Coalition: Gill Watt - *Chairman of the LPC, AMD, Boston, MA*
- II. Overview of CPF: Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*
- III. Convergence Activities with other Power-Aware Formats: Gary Delp - *LSI Logic Corp., Rochester, MN*
- IV. Library Considerations for Low Power: Rob Aitken - *ARM Ltd, Sunnyvale, CA*
- V. End-user Experiences: Herve Menager - *NXP, San Jose, CA*
- VI. EDA Tool Developers for Low Power: Dave Allen - *Atrenta, San Jose, CA*; Devadas Varma, *Calypto Design Systems, Inc., Santa Clara, CA* and Tom Miller - *Sequence Design, Inc., Santa Clara, CA*
- VII. Panel Discussion (all presenters)

**Workshop Agenda: Design and Verification of Low Power ICs  
Sunday, June 3, 2007, 4:00 - 7:00 p.m. | Room: 6E**

- I. Introduction: Yatin Trivedi - *Director, Industry Partnership Program, Magma Design Automation, Inc., San Jose, CA*
- II. Customer Perspective: David Peterman - *Manager, Wireless Terminals Business Unit EDA, Texas Instruments Inc., Dallas, TX*
- III. Brief History of Low Power Standards: Shrenik Mehta - *Accellera Chair; Senior Director, Frontend Technologies & OpenSPARC Program, Sun Microsystems, Inc., Sunnyvale, CA*; Edward Rashba - *Director, New Business Ventures, IEEE Standards Association, Piscataway, NJ*
- IV. Technical Content of Low Power Standard: Stephen Bailey - *Product Marketing Manager, Verification, Mentor Graphics Corp., Wilsonville, OR* and Gary Delp - *Distinguished Engineer, LSI Logic Corp., Rochester, MN*
- V. Low Power Solution Flow for Design and Verification: Mike Keating, *Synopsys Fellow, Synopsys, Inc., Mountain View, CA*; Juergen Karmann - *Senior Staff Engineer Design Methodology, Automotive, Industrial & Multimarket, Infineon Technologies AG, Munich, Germany*
- VI. Interoperability in Action: A Multi-Vendor Collaborative Solution
- VII. Roundtable and Wrap-up

**Registration**

Workshop registration is available online now in the registration section of the DAC Web site at [www.dac.com](http://www.dac.com). The registration fee for each workshop is \$75 for ACM and IEEE members, \$100 per person for non-members. Workshop registration is not included in DAC conference registration, nor is conference registration required to attend any of the workshops.

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## **About DAC**

The Design Automation Conference (DAC) is the premier educational and networking event for Electronic Design Automation (EDA) and silicon solutions. More than 11,000 designers, developers, researchers, academics and managers from leading electronics companies and universities from around the world attend. DAC features close to 60 technical sessions covering the latest research on design methodologies and technologies, EDA tool developments and trends selected by a diverse committee of electronic design experts. A highlight is its Exhibition and Suite area with approximately 250 of the leading and emerging EDA, silicon and IP providers. More details about DAC are available at: [www.dac.com](http://www.dac.com).

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