



FOR IMMEDIATE RELEASE

News Release

For more information, please contact:
Public Relations for DAC:
Emily Taylor, Weber Shandwick
(503) 552-3732
etaylor@webershandwick.com

44th Design Automation Conference to Offer Six Hands-on-Tutorials on DFM

BOULDER, Colo. — May 10, 2007 — The Design Automation Conference (DAC), the electronic design automation (EDA) industry's premier event, will offer six Hands-on-Tutorials on design-for-manufacturing (DFM), throughout the conference, to be held June 4 - 8 at the San Diego Convention Center in San Diego, Calif. The tutorials will provide design engineers valuable, in-depth, technical training on various aspects of DFM, one of today's most challenging design areas.

The registration fee for the tutorials is \$75 per tutorial and includes hands-on computer training, coffee breaks and tutorial notes. Attendees can register for the conference, including these tutorials, online at the DAC Web site <http://www.dac.com/44th/reg.html> or at the conference. Attendees may register for tutorials up to the start of the events but space is limited to the first 30 people.

Hands-on-Tutorials:

Standard Cell Library and Hard IP Design

Monday, June 4, 2007 from 9 a.m. to 12 p.m. in Room 11A

This tutorial, presented by Blaze DFM, Inc., Ponte Solutions, Inc. and Sagantec Solutions, Inc., addresses the designing of standard cells and other hard IP to minimize

—more—

manufacturing issues. Tutorial participants will learn how critical area analysis (CAA) and lithography simulation are used in concert with layout optimization to identify and repair weak spots in the layout that can harm yield.

Design for Manufacturing Variability with Confidence

Monday, June 4, 2007 from 2 to 5 p.m. in Room 11A

In this tutorial presented by Clear Shape Technologies, Inc., Cadence Design Systems, Inc., Texas Instruments Inc. and United Microelectronics Corp., technology leaders in chip design, semiconductor manufacturing, physical implementation and DFM analysis will discuss the intricacies of dealing with systematic variations and deliver a practical solution to the variability challenge with sub-90 nm technologies.

Deploying Statistical Timing -- from Characterization to Analysis and Optimization

Tuesday, June 5, 2007 from 2 to 5 p.m. in Room 11A

Presented by Altos Design Automation and Cadence Design Systems, Inc., this tutorial will contrast the results of performing analysis and optimization using both traditional corner-based static timing analysis (STA), and statistical static timing analysis (SSTA) on a given design to provide practical experience of the complete SSTA design methodology and a detailed understanding of its key advantages.

Approaching Yield in the Nanometer Age: The Framework for an Extensible DFM Methodology

Wednesday, June 6, 2007 from 9 a.m. to 12 p.m. in Room 11A

This tutorial, presented by Mentor Graphics Corp., Chartered Semiconductor Manufacturing, Sierra Design Automation, Inc. and ARM Ltd., will go into detail on the technical challenges and solutions required for DFM in the nanometer era, looking at both the business and historical context of the IC design and manufacturing process.

Manufacturing Aware Optimization

Wednesday, June 6, 2007 from 2 to 5 p.m. in Room 11A

—more—

This hands-on tutorial presented by Blaze DFM, Inc. and Taiwan Semiconductor Manufacturing Company, Ltd. will address the topic of manufacturing variations and their impact on the design flow. It covers approaches for modeling and predicting manufacturing variations, and using the predicted manufacturing variation data to optimize designs using novel electrical DFM techniques.

Timing Closure: Requirements for Variation Aware Design

Thursday, June 7, 2007 from 9 a.m. to 12 p.m. in Room 11A

In this tutorial, presented by Extreme DA Corp., Texas Instruments Inc., PDF Solutions and United Microelectronics Corp., the audience will be introduced to the components of a next-generation timing analysis methodology. Practical examples will be given, starting with front-end and back-end process characterization that captures variability statistics of systematic and random variations and experiences from foundry, IDM, and EDA perspectives will be included.

About DAC

The Design Automation Conference (DAC) is the premier educational and networking event for Electronic Design Automation (EDA) and silicon solutions. More than 11,000 designers, developers, researchers, academics and managers from leading electronics companies and universities from around the world attend. DAC features close to 60 technical sessions covering the latest research on design methodologies and technologies, EDA developments and trends selected by a diverse committee of electronic design experts. A highlight is its Exhibition and Suite area with approximately 250 of the leading and emerging EDA, silicon and IP providers. More details are available at: www.dac.com.

###