

Call for Papers

46th DESIGN AUTOMATION CONFERENCE®

Moscone Convention Center, San Francisco CA • July 26-31, 2009

FOR INFORMATION CALL: 1-303-530-4333

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Five types of submissions are invited: regular papers, "Wild and Crazy Ideas" (WACI) topic papers, special sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. Panel and tutorial suggestions, and special session submissions are due no later than 5:00pm MST, November 3, 2008; regular papers and WACI papers are due no later than 5:00pm MST, December 19, 2008.

Topics of Interest

DAC 2009 is seeking papers that deal with tools, algorithms and design techniques for all aspects of electronic circuit design. Apart from these core Electronic Design Automation topics, we are specifically soliciting papers in several focus areas. These include multi-core applications in design automation, embedded system and wireless design, high level design, IP design, new technologies, technology CAD, fab automation, as well as packaging and beyond-the-die design. In addition, our "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even unproven) technical ideas that create a buzz and get people talking. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees. Students worldwide are invited to submit their work for the design contest.

All Submissions must be made electronically at the DAC website, www.dac.com

Regular Paper Submissions Are Due Before 5:00pm MST, December 19, 2008

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and with any references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. Format templates are available on the DAC website for your convenience. WACI submissions may be no longer than two pages. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences and symposia in the field to check for double submissions. Additional submission guidelines will be available on the DAC website after September 3, 2008. All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage, except for submissions to WACI. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in on the DAC website after March 26, 2009. Complete author kits will be sent via email by April 6, 2009.

WACI Paper Submissions Are Due Before 5:00pm MST, December 19, 2008

Submissions to the Wild and Crazy Ideas track should not exceed two pages. Otherwise, they must follow the above rules and deadlines for the regular papers. A regular DAC paper explores a specific technology problem and proposes a complete solution to it, with a full table of results. In contrast, a WACI paper would present less developed, but highly innovative ideas related to areas relevant to DAC.

Special Session Submissions Are Due Before 5:00pm MST, November 3, 2008

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. As the term implies, a special session covers an entire session on a special topic. This requires at least three inspiring speakers who address the topic from different angles. The topic must represent an emerging area that does not yet receive sufficient focus from regular papers. DAC reserves the right to restructure all special sessions.

Panel and Tutorial Submissions Are Due Before 5:00pm MST, November 3, 2008

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals.

Student Design Contest Submissions Are Due Before 5:00pm, MST, December 8, 2008

Students are invited to submit descriptions of original electronic designs, either circuit level or system-level. Accepted contributions will be published in the proceedings and presented at DAC 2009. Therefore this is an excellent opportunity to showcase your design work to the world. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) provide a complete description of the project, and (5) be no more than six pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2007. Submitted designs should not have received awards in other contests. Detailed rules and guidelines for all submissions are available on the DAC website.

Submitters are required to specify a category from the following LIST

1. System-level Design and Co-design

- 1.1 System specification, modeling, simulation, and performance analysis
- 1.2 Scheduling, HW-SW partitioning, HW-SW interface synthesis
- 1.3 IP and platform-based design, IP protection
- 1.4 System-on-Chip (SoC) and Multiprocessor SoC (MPSoC)
- 1.5 Application-specific processor design tools

2. System-level Communication and Networks on Chip

- 2.1 Modeling and performance analysis
- 2.2 Communications-based design, communication and network synthesis
- 2.3 Architectural synthesis, mapping, routing, scheduling
- 2.4 Optimization for energy, fault-tolerance, reliability
- 2.5 Interfacing and software issues, Beyond-the-die communication
- 2.6 NoC Design methodologies, case studies and prototyping

3. Embedded Hardware Design and Applications

- 3.1 Case studies of embedded system design
- 3.2 Flows and methods for specific applications and design domains

4. Embedded Software Tools and Design

- 4.1 Retargetable compilation
- 4.2 Memory/cache optimization
- 4.3 Real-time single - and multi-processor scheduling, linking, loading
- 4.4 Real-time operating systems

5. Power Analysis and Low-power Design

- 5.1 System-level power design and thermal management

- 5.2 Embedded low-power approaches: partitioning, scheduling, and resource management

- 5.3 High-level power estimation and optimization

- 5.4 Gate-level power analysis and optimization

- 5.5 Device and circuit techniques for low-power design

- 5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. Verification

- 6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design

- 6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking

- 6.3 Emulation and hardware simulators or accelerator engines

- 6.4 Modeling languages and related formalisms, verification plan development and implementation

- 6.5 Assertion-based verification, coverage analysis, constrained-random testbench generation

7. High-level Synthesis, Logic Synthesis and Circuit Optimization

- 7.1 Combinational, sequential, and asynchronous logic synthesis

- 7.2 Library mapping, cell-based design and optimization

- 7.3 Transistor and gate sizing and resynthesis

- 7.4 Interactions between logic design and layout or physical synthesis

- 7.5 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods

- 7.6 Resource scheduling, allocation, and Synthesis

8. Circuit, Interconnect and Manufacturing Simulation and Analysis

- 8.1 Electrical-level circuit simulation
- 8.2 Model-order reduction methods for linear systems
- 8.3 Interconnect and substrate modeling and extraction
- 8.4 High-frequency and electromagnetic simulation of circuits
- 8.5 Thermal and electrothermal simulation
- 8.6 Technology CAD and fab automation

9. Timing Analysis

- 9.1 Process technology characterization, and modeling
- 9.2 Deterministic static timing analysis and verification
- 9.3 Statistical performance analysis and optimization

10. Physical Design and Manufacturability

- 10.1 Physical floorplanning, partitioning, placement
- 10.2 Buffer insertion, routing, interconnect planning
- 10.3 Physical verification and design rule checking
- 10.4 Automated synthesis of clock networks
- 10.5 Reticle enhancement, lithography-related design optimizations
- 10.6 Design for manufacturability, yield, defect tolerance, cost issues, and impacts of DFM
- 10.7 3-D circuit design and algorithms
- 10.8 System-in-Package design, Chip-package-board codesign
- 10.9 Design for resilience under manufacturing variations

11. Signal Integrity and Design Reliability

- 11.1 Signal integrity, capacitive and inductive crosstalk
- 11.2 Reliability modeling and analysis
- 11.3 Novel clocking and power delivery schemes
- 11.4 Power grid robustness analysis and optimization
- 11.5 Soft errors and single-event upsets (SEUs)
- 11.6 Thermal reliability

12. Analog/Mixed-signal and RF

- 12.1 Analog, mixed-signal, and RF design methodologies
- 12.2 Automated synthesis and macromodeling
- 12.3 Analog, mixed-signal and RF simulation and optimization

- 12.4 High-frequency design and advanced antenna design for wireless

13. FPGA Design Tools and Applications

- 13.1 Rapid prototyping
- 13.2 Logic synthesis and physical design techniques for FPGAs
- 13.3 Configurable and reconfigurable computing

14. Testing

- 14.1 Test quality/reliability, current-based test, delay test, low power test
- 14.2 Digital fault modeling, automatic test generation, fault simulation
- 14.3 Digital design-for-test, test data compression, built-in self test
- 14.4 Memory test and repair, FPGA testing
- 14.5 Fault tolerance and on-line testing
- 14.6 Analog/mixed-signal/RF testing, System-in-Package (SiP) testing
- 14.7 Board - and system-level test, System-on-Chip (SoC) testing
- 14.8 Silicon debug, diagnosis, post-silicon design validation

15. New and Emerging Design Technologies, including but not restricted to

- 15.1 MEMS, sensors, actuators, imaging devices
- 15.2 Nanotechnologies, nanowires, nanotubes
- 15.3 Quantum computing
- 15.4 Biologically based or biologically inspired systems
- 15.5 Stacked devices for 3-D design, new transistor structures and devices, new or radical process technologies
- 15.6 Optical devices and communication

16. Cutting-edge Circuit Design and IP

- 16.1 Standard cell libraries and IP building blocks
- 16.2 I/O circuitry for high-speed communication
- 16.3 Design methodologies using IP blocks
- 16.4 Design flows for advanced SoC integration

17. Wild and Crazy Ideas

We invite papers with genuinely forward-looking, radical and innovative ideas in the area of electronic design or electronic design automation. Concepts that stimulate discussion are welcome candidates. Research that incrementally improves on prior work is not suited for this category.