



DESIGN AUTOMATION CONFERENCE

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46th Design Automation Conference Goes Green at Moscone This Week

SAN FRANCISCO – July 27, 2009 – The 46th Design Automation Conference ([DAC](#)), being held this week at the Moscone Center, will include several events exploring the “green” side of the electronics design industry, including two Pavilion Panels on Wednesday, and a special plenary panel, a technical panel and a special session on Thursday. Attendees will be able to learn about low-power chip design methods and hear discussions of the environmental impact of electronics manufacturing and the potential benefits of green technology for the industry.

Fittingly, the venue for this year’s DAC, Moscone Center, was recently recognized by the Environmental Protection Agency as the Pacific Region’s 2009 Sustainable Facility for its operations practices, including recycling, zero-waste catering and solar energy generation.

The community-selected topic [“Power Scavenging: Waste Not, Want Not”](#) for a special Pavilion Panel on Wednesday – 10 to 10:45 a.m. in Booth #1928 – reflects the growing interest in low-power chip design, which is driven in part by environmental concerns. John Blyler, editor-in-chief of Chip Design Magazine, will moderate this panel discussion about methods of harnessing hidden power for today’s complex applications.

Panelists:

Sandip Kundu – University of Massachusetts, Amherst, Amherst, Mass.

Steve Grady – Cymbet Corp., Elk River, Minn.

Mark Buccini – Texas Instruments, Inc., Dallas, Texas

press release

On Wednesday from 12:30 to 1:30 p.m. in Booth #1928, Carl Guardino, CEO of the Silicon Valley Leadership Group, will moderate a Pavilion Panel discussion, [“Electronics Going Green: Future or Futile?”](#) Three experts will consider whether the electronics industry is collectively doing enough to improve environmental responsibility, and what more can be done.

Panelists:

Doug Johnson – Consumer Electronics Association, Washington, DC

Scott Mattoon – Sun Microsystems, Inc., San Francisco, Calif.

Bruce S. Klafter – Applied Materials, Inc., Santa Clara, Calif.

In addition, there will be a special plenary panel titled [“How Green is My Silicon Valley.”](#) on Thursday, July 30, from noon to 1:45 p.m. Moderated by Walden C. Rhines, chairman and CEO, Mentor Graphics Corp. and EDA Consortium chair, this panel will explore the implications of green technology innovation for the electronic design industry.

Panelists:

John A. “Skip” Laitner – American Council for an Energy-Efficiency Economy (ACEEE), Washington, DC

Thomas Jacoby – California Clean Energy Fund, Cupertino, Calif.

Peter Williams – IBM’s Big Green Innovation, San Francisco, Calif.

Dennis Buss – Texas Instruments, Dallas, Texas

Ian Wright – Wrightspeed, Inc., San Francisco, Calif.

A technical panel, “From Milliwatts to Megawatts: The System-Level Power Challenge”, will also take place on Thursday, July 30, from 2 p.m. to 4 p.m. Moderated by Rajesh Gupta of University of California San Diego, the panel will explore best practices and future opportunities for power optimization at the system level – and whether this will drive methodology change in system-level design.

Panelists:

Kimmo Kuusilinna – Nokia, Palo Alto, Calif.

Bradley McCredie – IBM Corp., Austin, Texas

Andres Takach – Mentor Graphics Corp., Wilsonville, Ore.

Jason Cong – University of California, Los Angeles, Calif.

Johannes Stahl – CoWare, Inc., Aachen, Germany

Finally, a special session titled “[Technologies for Green Data Centers](#),” is scheduled for Thursday, July 30, from 4:30 p.m. to 6 p.m. The session will be chaired by Prof. Massoud Pedram and describe state-of-the-art in computing, storage and networking technologies as well as data center design and operation. The speakers will focus on modeling data centers and managing the energy efficiency challenges in large data centers.

Speakers:

Randy H. Katz – University of California, Berkeley, Calif.

Prith Banerjee – Hewlett-Packard Co., Palo Alto, Calif.

Dilip D. Kandlur – IBM Corp., Austin, Texas

Registration

Attendance to the DAC Pavilion Panels and special plenary panel is included with both the Full Conference and Exhibit-Only registration options. For more details on DAC’s full program and to register, please visit www.dac.com.

About DAC

The Design Automation Conference (DAC) is recognized as the premier event for the design of electronic circuits and systems, and for Electronic Design Automation (EDA) and silicon solutions. A diverse worldwide community representing more than 1,000 organizations attends each year, from system designers and architects, logic and circuit designers, validation engineers, CAD managers, senior managers and executives to researchers and academicians from leading universities. Close to 60 technical sessions selected by a committee of electronic design experts offer information on recent developments and trends, management practices and new products, methodologies and technologies. A highlight of DAC is its Exhibition and Suite area with approximately 200 of the leading and emerging EDA, silicon, IP and design services providers. The conference is sponsored by the Association for Computing Machinery (ACM), the Electronic Design Automation Consortium (EDA Consortium), and the Institute of Electrical and Electronics Engineers (IEEE), and is supported by ACM's Special Interest Group on Design Automation (SIGDA) and IEEE’s Council on Electronic Design Automation (CEDA), Circuits

and Systems Society (CASS), and Computer-Aided Network Design (CANDE) Committee.
More details are available at: www.dac.com.

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