



DESIGN AUTOMATION CONFERENCE

For more information, please contact:

Emily Taylor
Weber Shandwick
+1 503.552.3733
etaylor@webershandwick.com

46th DAC Announces Keynote Speakers and Special Monday Keynote Panel

Fu-Chieh Hsu of TSMC and Bill Dally of NVIDIA to Address Futures for Electronic Design

Special Monday Keynote Panel to Feature CEOs of Cadence, Mentor Graphics and Synopsys

LOUISVILLE, Colo. – May 20, 2009 – The 46th Design Automation Conference (DAC) today announced its keynote sessions, featuring technology and business luminaries from the electronics industry. Fu-Chieh Hsu, Vice President, Design and Technology Platform of Taiwan Semiconductor Manufacturing Company (TSMC) will deliver the Tuesday Keynote, entitled “Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models” at 8:30 a.m. on July 28. Bill Dally, Chief Scientist, NVIDIA Corporation will deliver the Wednesday Keynote on “The End of Denial Architecture and the Rise of Throughput Computing” at 11:15 a.m. on July 29. In a special Monday Keynote Panel, “Futures for EDA: The CEO View,” Lip-Bu Tan of Cadence Design Systems, Inc., Walden C. Rhines of Mentor Graphics Corp. and Aart J. de Geus of Synopsys, Inc. will discuss industry futures with respect to markets, business and technology at 4:30 p.m. on July 27. [DAC](#) will take place July 26 – 31, 2009 at Moscone Center in San Francisco.

“DAC is delighted to welcome these distinguished technology and business leaders as our keynote speakers this year,” said Andrew B. Kahng, General Chair of the 46th DAC Executive Committee. “Each has provided inspiration and vision to our industry throughout multiple successful careers as technologist, business leader, and entrepreneur. Dr. Hsu has a truly unique perspective on future business models for design, manufacturing and the overall semiconductor industry. Dr. Dally’s

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work has made throughput-optimized processing a reality, and his vision for future architectures as well as EDA challenges and opportunities is certain to be of great interest to attendees.”

Fu-Chieh Hsu’s keynote will focus on the new complexity barrier facing the semiconductor industry. He will discuss how the industry’s key challenges are no longer discrete issues that can be addressed by point-tool solutions, but instead demand new breakthrough technologies and integrated EDA solutions. His talk will outline a new collaborative business model that is part of the solution required for the IC design and manufacturing ecosystem to collectively meet these emerging challenges.

Bill Dally will address the future of throughput-optimized processors, such as graphics processing units (GPUs), which today have hundreds of cores and will have thousands of cores by 2015. He will describe challenges and opportunities for the EDA world that are inherent in the architecture and programming of future throughput processors, and also give examples of exploiting parallelism and locality drawn from the Imagine and Merrimac projects, from NVIDIA GPUs, and from three generations of stream programming systems.

In the keynote panel, leading EDA CEOs Aart de Geus of Synopsys, Inc., Walden C. Rhines of Mentor Graphics Corp. and Lip-Bu Tan of Cadence Design Systems, Inc. will share their views on the outlook for EDA in light of the current economic climate and the perennial challenges faced by the industry. The panel will be moderated by Juan-Antonio Carballo, a partner with IBM Venture Capital Group and Worldwide Manager, IBM Microelectronics Services.

Speaker Biographies

Fu-Chieh Hsu, Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC)

Dr. Fu-Chieh Hsu has served as Vice President of Design and Technology Platform for TSMC since April 2006. He is responsible for all design service operations at TSMC and works with the Marketing and R&D departments to provide customers with technology platform solutions.

Dr. Hsu founded Monolithic System Tech. Inc. (MoSys) in 1991 and served as its Chairman and Chief Executive Officer until retiring at the end of 2004. He was Chairman and President of Myson Technology Inc. (now Myson Century Inc.) from 1990 to 1991. Prior to that, Dr. Hsu

worked at Integrated Device Tech. Inc. as Chief Technology Officer and Vice President as well as other senior positions. Dr. Hsu also served at Hewlett-Packard Labs.

Dr. Hsu has published or contributed to more than 40 papers and also holds 55 U.S. patents. Dr. Hsu received his Bachelor of Science degree in electrical engineering from the National Taiwan University in 1978, and Master of Science and Ph.D. degrees in electrical engineering and computer sciences from University of California, Berkeley, in 1981 and 1983, respectively.

Bill Dally, NVIDIA

Bill Dally joined NVIDIA in January 2009 as chief scientist, after spending 12 years at Stanford University, where he was chairman of the computer science department. Dally and his Stanford team developed the system architecture, network architecture, signaling, routing and synchronization technology that is found in most large parallel computers today.

Dally was previously at the Massachusetts Institute of Technology from 1986 to 1997, where he and his team built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanism from programming models and demonstrated very low overhead synchronization and communication mechanisms. From 1983 to 1986, he was at California Institute of Technology (CalTech), where he designed the MOSSIM Simulation Engine and the Torus Routing chip, which pioneered “wormhole” routing and virtual-channel flow control.

Dally is a cofounder of Velio Communications and Stream Processors. He is a member of the National Academy of Engineering, a Fellow of the American Academy of Arts & Sciences, a Fellow of the IEEE and the ACM, and has received the IEEE Seymour Cray Award and the ACM Maurice Wilkes award. He has published over 200 papers, holds over 50 issued patents, and is an author of two textbooks.

He received a bachelor’s degree in Electrical Engineering from Virginia Tech, a master’s in Electrical Engineering from Stanford University and a Ph.D. in Computer Science from CalTech.

About DAC

The Design Automation Conference (DAC) is recognized as the premier event for the design of electronic circuits and systems, and for Electronic Design Automation (EDA) and silicon solutions. A diverse worldwide community representing more than 1,000 organizations attends each year, from system designers and architects, logic and circuit designers, validation engineers, CAD managers, senior managers and executives to researchers and academicians from leading universities. Close to 60 technical sessions selected by a committee of electronic design experts offer information on recent developments and trends, management practices and new products, methodologies and technologies. A highlight of DAC is its Exhibition and Suite area with approximately 200 of the leading and emerging EDA, silicon, IP and design services providers. The conference is sponsored by the Association for Computing Machinery (ACM), the Electronic Design Automation Consortium (EDA Consortium), and the Institute of Electrical and Electronics Engineers (IEEE). In addition, the conference is supported by ACM's Special Interest Group on Design Automation (SIGDA), IEEE's Council on Electronic Design Automation (CEDA), Circuits and Systems Society (CASS), and Computer Aided Network Design (CANDE). More details are available at: www.dac.com.

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