



DESIGN AUTOMATION CONFERENCE

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46th Design Automation Conference Offers Six Full-Day Tutorials
Participants Can Earn Continuing Education Credits

LOUISVILLE, Colo. – June 22, 2009 – The Design Automation Conference (DAC) will offer six educational, full-day tutorials focused on a variety of design methods. The full-day tutorials will be held Monday, July 27 and Friday, July 31 at this year’s DAC. The tutorials will provide CAD professionals, design engineers, their management, as well as academic researchers with an in-depth look at some of the most challenging and topical areas of electronic design, as industry professionals and experts address key trends and issues facing today’s EDA industry. This year, tutorial attendees have the opportunity to earn university [Continuing Education Credits](#) in the field of VLSI and Design Automation through new partnerships between DAC and the University of California Santa Cruz (UCSC) Extension, and the University of California San Diego (UCSD) Extension. The [46th DAC](#) will be held July 26 – 31 at the Moscone Center in San Francisco.

“The full-day tutorials are an important part of DAC that offer participants the opportunity to explore a subject in-depth and gain valuable, practical knowledge,” said Dennis Sylvester, 46th DAC Tutorial Chair. “This year we’re excited to partner with two UC campuses to offer tutorial participants the opportunity to earn university credit for their work.”

Full-Day Tutorials

[Low-Power SOC Design: State of the Art and Directions](#)

Monday, July 27: 8:30 a.m. – 4:30 p.m.

press release

This tutorial will focus on industrial case studies that highlight state-of-the-art techniques to achieve improved energy efficiency, with special emphasis on aggressive scaling of the power supply. Practical challenges will be discussed, such as early power estimation at the architectural level, power verification along the design flow, timing characterization when using dynamic voltage/frequency scaling (DVFS) and power gating with retentive sequential elements.

Instructors:

Kaushik Roy – *Purdue University, West Lafayette, Ind.*

Mike Keating – *Synopsys, Inc., Mountain View, Calif.*

Bernard Ramanadin – *STMicroelectronics, Crolles, France*

Matt Severson – *Qualcomm CDMA Technologies, Inc., San Diego, Calif.*

[High-Level Synthesis for ESL Design: Fundamentals and Case Studies](#)

Monday, July 27: 8:30 a.m. – 4:30 p.m.

Attendees participating in this tutorial will learn about High-Level Synthesis techniques they can use immediately. They will also examine the use and impact of High-Level Synthesis on the design process, from conception through implementation. At the conclusion of the tutorial, attendees also will have gained insight into the long-term direction the industry will take.

Instructors:

Daniel Gajski – *University of California, Irvine, Calif.*

Jason Cong – *University of California, Los Angeles, Calif.*

Nitin Chawla – *STMicroelectronics, Greater Noida, India*

Sumio Morioka – *NEC Corp., Kawasaki, Japan*

Rodric Rabbah – *IBM Corp., Hawthorne, N.Y.*

Scott Mahlke – *University of Michigan, Ann Arbor, Mich.*

[Post-Silicon Validation and Runtime Verification: Ensuring Correctness after First Silicon](#)

Friday, July 31: 9 a.m. – 5 p.m.

This tutorial will address leading-edge methods for detecting and correcting bugs after the first few silicon prototypes of a design become available. It is intended for microprocessor architects and designers, verification engineers, and CAD professionals interested in a better understanding of current post-silicon validation technologies. It will also benefit designers and verification experts in providing an overview of runtime verification solutions that have recently been proposed by the research community.

Instructors:

Valeria Bertacco – *University of Michigan, Ann Arbor, Mich.*

Rand Gray – *Intel Corp., Hillsboro, Ore.*

Jai Kumar – *Sun Microsystems, Inc., Santa Clara, Calif.*

Albert Meixner – *NVIDIA Corp., Santa Clara, Calif.*

Bart Vermeulen – *NXP Semiconductors, Eindhoven, The Netherlands*

[CAD: Utilizing the State of the Art, and Beyond, in Parallel Programming](#)

Friday, July 31: 9 a.m. – 5 p.m.

Participants in this tutorial first will be introduced to the state-of-the-art in parallel programming and a number of the most commonly used languages will be introduced, including pThreads, OpenMP, Thread-Building Blocks and MPI. Later, participants will be given an overview of the latest approaches in applying these technologies to CAD.

Instructors:

Kurt Keutzer – *University of California, Berkeley, Calif.*

Tim Mattson – *Intel Corp., DuPont, Wash.*

Tom Spyrou – *Cadence Design Systems, Inc., San Jose, Calif.*

Michael Wrinn – *Intel Corp., Hillsboro, Ore.*

[From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials](#)

Friday, July 31: 9 a.m. – 5 p.m.

This tutorial will focus on nanoscale devices and will address major existing nanosystems design principles and identify the key challenges and solutions for bridging the gap between nanodevice research and nanosystem building. The tutorial will conclude with insights for attendees regarding future nanoscale device and nanoscale system research.

Instructors:

Yong Chen – *University of California, Los Angeles, Calif.*

André DeHon – *University of Pennsylvania, Philadelphia, Pa.*

Stuart Parkin – *IBM Corp., San Jose, Calif.*

Subhasish Mitra – *Stanford University, Palo Alto, Calif.*

Deming Chen – *University of Illinois, Urbana-Champaign, Ill.*

[Functional Verification Planning and Management: Navigating from Specification to Functional Closure](#)

Friday, July 31: 9 a.m. – 5 p.m.

This tutorial will teach advanced methods for planning, monitoring and assessing verification progress, each an essential step for achieving predictable, successful verification. Attendees will discuss how to choose design features that are candidates for verification using each of these techniques so that the overall verification labor is minimized while verification completeness is maximized.

Instructors:

Andrew Piziali – *Consultant, Parker, Texas*

Avi Ziv – *IBM Corp., Haifa, Israel*

Janick Bergeron – *Synopsys, Inc., Ottawa, Canada*

DAC Tutorials and Continuing Education Credits

All DAC Tutorial sessions are reviewed and approved by UC Extension to confirm that participants will be eligible for CEU credits. For more information on the University of California Santa Cruz (UCSC) Extension program, visit <http://www.ucsc-extension.edu/view/engineering/DAC>, and for more details on the University of California San Diego (UCSD) Extension program, visit <http://extension.ucsd.edu/icdesign>. For more information, or to register for credit, visit http://www.dac.com/46th/tut_credit.html.

Registration

The registration fee for each tutorial is \$200 for student ACM and IEEE members, \$300 for ACM and IEEE members and \$400 for non-members and includes a continental breakfast, lunch, coffee breaks and tutorial notes. The advance conference registration discount deadline is June 29, 2009. For more details on DAC's full-day tutorials, and to register, please visit www.dac.com.

About DAC

The Design Automation Conference (DAC) is recognized as the premier event for the design of electronic circuits and systems, and for Electronic Design Automation (EDA) and silicon solutions. A diverse worldwide community representing more than 1,000 organizations attends each year, from system designers and architects, logic and circuit designers, validation engineers, CAD managers, senior managers and executives to researchers and academicians from leading universities. Close to 60 technical sessions selected by a committee of electronic design experts offer information on recent developments and trends, management practices and new products, methodologies and technologies. A highlight of DAC is its Exhibition and Suite area with approximately 200 of the leading and emerging EDA, silicon, IP and design services providers. The conference is sponsored by the Association for Computing Machinery (ACM), the Electronic Design Automation Consortium (EDA Consortium), and the Institute of Electrical and Electronics Engineers (IEEE), and is supported by ACM's Special Interest Group on Design

Automation (SIGDA) and IEEE's Council on Electronic Design Automation (CEDA), Circuits and Systems Society (CASS), and Computer-Aided Network Design (CANDE) Committee.

More details are available at: www.dac.com.

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