



DESIGN AUTOMATION CONFERENCE

For more information, please contact:

Emily Taylor
Weber Shandwick
+1 503.552.3733
etaylor@webershandwick.com

Designers to Share Real-World Experiences at the 46th Design Automation Conference User Track

More Than 80 Technical Presentations and Posters from Top Designers at Intel, STMicroelectronics, Qualcomm and More

LOUISVILLE, Colo. – June 25, 2009 – The 46th Design Automation Conference (DAC) technical program will include a new [User Track](#), featuring over 80 technical papers and posters presented by designers from around the world who will share their experiences creating today’s most complex chips. The User Track will cover the latest innovations in tool use and design methodologies across the entire design process, from system design exploration and embedded software synthesis in the front-end, to constraint generation and physical verification in the back-end. The User Track submissions were reviewed by a 20-member industry user committee who selected the 40 technical presentations that will be delivered, and the more than 40 additional presentations included in the poster session on Wednesday, July 29 from 1:30 p.m. – 3 p.m. The [46th DAC](#) will be held July 26 – 31, 2009, at the Moscone Center in San Francisco, CA.

“The User Track at DAC will provide designers a unique opportunity to learn, directly from other designers, how design tools can be applied successfully to solve complex design problems,” said Leon Stok of IBM, Co-Chair of the User Track.

Soha Hassoun of Tufts University, the other User Track Co-Chair added, “Based on the incredible industry response and exciting lineup of presentations, we anticipate that User Track will be a very valuable part of DAC this year for all who participate.”

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press release

The User Track includes nine sessions spread over three days, from Tuesday, July 28 through Thursday, July 30. The sessions will cover the full range of front and back-end design processes from power planning and analysis in the front-end to real-world timing analysis in the back-end.

A session on [Front-End Power Planning and Analysis](#) will include a presentation from a team at NEC Corp. on their use of an automated flow to pre-characterize the power consumption of a set of basic components, starting from their behavioral description in C down to their power estimation at the gate netlist level. A team from Cisco Systems Inc. will describe the use of a power noise analysis tool to analyze system power integrity. Intel engineers from India and Israel will discuss using abstract executable models to verify power management protocols.

In the [Timing Analysis in the Real World](#) session, users representing Atmel Corp, the European Space Agency, FishTail Design Automation, Fujitsu, IBM Corp., Sun Microsystems, Inc. and Texas Instruments, Inc. will share their successful analysis methodologies that lead to timely sign-off. They will address issues related to mixing gate-level and transistor-level timing analysis, applying statistical timing to processor design, effectively merging timing constraints from multiple domains, modeling network variation, and accounting for single event upsets.

In the [Practical Physical Design](#) session, a team from Intel will discuss effective and practical solutions to the ongoing challenge of logic changes that come in late in the development process. A team from Qualcomm, Inc. will describe automation in their semi-custom methodology for the design of the register arrays that are increasingly important to modern designs. Finally, STMicroelectronics engineers will share how they use IP-XACT standard from SPIRIT to enable IP reuse.

The [Advances in Analog and Mixed-Signal](#) session will include presentations from designers at Stanford University, Rambus Inc. and NetLogic Microsystems Inc. on how they have tackled the need for reuse with analog designs. In other presentations, a group from Cadence Design Systems, Inc. and National Chiao Tung University will explain their approach to integrating MEMs in mixed-signal designs, and a team from SySDSsoft, Inc. and Mentor Graphics Corp. will explain how their approach integrates physical design with electrical verification.

User Track Poster Session

The [User Track Poster Session](#), on Wednesday July 29 from 1:30 – 3 p.m., will feature approximately 40 posters on topics that span both front-end and back-end design. The session will include an Ice Cream Social and will provide an opportunity for informal personal interaction with EDA tool users from many leading companies.

Registration

Registration for the User Track is available for \$175 for ACM/IEEE members and \$225 for non-members. In addition, full-conference registration includes access to the User Track, the technical paper sessions, exhibits, and more. The deadline for advance registration discount is June 29, 2009. To register for DAC, visit www.dac.com or call 1-800-321-4573 in the U.S. to request registration materials.

About DAC

The Design Automation Conference (DAC) is recognized as the premier event for the design of electronic circuits and systems, and for Electronic Design Automation (EDA) and silicon solutions. A diverse worldwide community representing more than 1,000 organizations attends each year, from system designers and architects, logic and circuit designers, validation engineers, CAD managers, senior managers and executives to researchers and academicians from leading universities. Close to 60 technical sessions selected by a committee of electronic design experts offer information on recent developments and trends, management practices and new products, methodologies and technologies. A highlight of DAC is its Exhibition and Suite area with approximately 200 of the leading and emerging EDA, silicon, IP and design services providers. The conference is sponsored by the Association for Computing Machinery (ACM), the Electronic Design Automation Consortium (EDA Consortium), and the Institute of Electrical and Electronics Engineers (IEEE), and is supported by ACM's Special Interest Group on Design Automation (SIGDA) and IEEE's Council on Electronic Design Automation (CEDA), Circuits and Systems Society (CASS), and Computer-Aided Network Design (CANDE) Committee. More details are available at: www.dac.com.

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