Chip - Package - PC Board Co-Design:

Applying a Chip Power Model in System Power Integrity Analysis

Authors:
Rick Brooks, Cisco, ricbrook@cisco.com
Jane Lim, Cisco, honglim@cisco.com
Udupi Harisharan, Cisco, uharisha@cisco.com
Agenda

- Introduction and problem statement
- CPM™ - reduced order die models for Chip Package System analysis
  - Concepts and steps in creating a model
  - Validation of the model
  - Applications of CPM
- **Case study**: Use of CPM for system and package level power delivery network analysis and validation for a Cisco product.
Introduction and Problem Statement

• The power integrity of a chip when mounted on a package and PC board is often not well understood during the chip design phase.
• Traditional system power integrity analysis has often been limited to considering DC IR drop only.
• How can we insure a robust power integrity design while not over designing the board, package and die?
• The goal is to have a power integrity methodology that helps to predict system level behavior while in the design phase.
• One problem is getting good models of die current behavior based on the actual logic and the nature of the die power network.
• One way to get a model from an actual die during the design phase is from Apache RedHawk, the CPM™ or Chip Power Model.
CPM™ Equivalent Circuit

For each domain:
- \( C_{\text{die}}/R_{\text{die}} \)
- \( I_{\text{cc}}(t) \) for every pin for VCD and VectorLess modes of switching

- Compact SPICE model for the full-chip PDN
- Enable the analysis, diagnostic and optimization of the system level power integrity design
- Full-chip time and frequency domain simulation and model order reduction
Case Study: Use of CPM in Cisco System Design

• Design description
  Die: 90nm ASIC with 32 Watt power consumption
  1 core VDD and 3 IO power domains,
  Including eDRAM, SerDes
  96 million core transistors
  Package: Flip-chip 33mm, 8 layer, 1020 BGA pins
  Board: 2-3mm thick PCB, Multi-layer (FR4)

• Analysis and design goals:
  Verify against noise targets at various parts of the PDN
  Set system level power performance expectations
  Validate for different operating modes of the ASICs
Analyses Done

For ASIC Validation

- Perform detailed ASIC level DC (static) and transient (dynamic voltage drop) analyses using RedHawk™
- Include package model for ASIC level sign-off
- Perform validation at every stage to tape-out
Analyses Done For System Validation

- Detailed system level AC and Transient analyses for different operating modes (multiple CPMs) of the ASIC
- AC analyses to understand impedance and resonance points for all power domains
- Transient analysis to ensure power integrity both at BGA pin and at die bumps for all power domains
Simulation Setup For System Validation

- Generic PC board power model
- S-parameter (or Broadband SPICE) based package model
- CPMs of the ASIC are created for different operating modes
- AC analysis also done with lumped model estimates
- Netlist simulated using Spice

System Schematic of Simulation Setup for Core VDD
Partitioning the Die and Package Models

- The Die, Package, and PC Board Models must be partitioned so that they map correctly to each other.
- In this example, the core VDD is divided into 36 partitions.
CPM Creation Example

- Using RedHawk/CPM to create pin group based die model
- VectorLess mode used to create switching scenarios
- Fully coupled network solve and reduction
- Precise time domain and frequency domain representation of the on-die noise source

<table>
<thead>
<tr>
<th>CPM</th>
<th>PVT</th>
<th>Chip Activity</th>
<th>Memory</th>
<th>Clock Gating</th>
<th>EDRAM Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model_A</td>
<td>Fast Process, High Voltage (1.05V), High Temperature</td>
<td>12.5%</td>
<td>30%</td>
<td>15%</td>
<td>50%</td>
</tr>
<tr>
<td>Model_B</td>
<td>Slow Process, Low Voltage (0.95V), High Temperature</td>
<td>12.5%</td>
<td>30%</td>
<td>15%</td>
<td>50%</td>
</tr>
</tbody>
</table>
CPM Self-consistency Checks

- Hook-up the S-param package model to the CPM and run in HSpice
- Measure the voltage drop at the package bump nodes and correlate to Redhawk full chip DvD results
CPM Self-consistency Checks

- Both fast and slow CPMs models were compared and validated

**CPM SPICE simulation waveforms (Die ports 1 to 72):**

<table>
<thead>
<tr>
<th>Model_A</th>
<th>Port #</th>
<th>Redhawk</th>
<th>CPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Si, High Voltage &amp; Temp</td>
<td>p20</td>
<td>32mV</td>
<td>33mV</td>
</tr>
<tr>
<td></td>
<td>p56</td>
<td>33mV</td>
<td>33mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Model_B</th>
<th>Port #</th>
<th>Redhawk</th>
<th>CPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow Si, Low Voltage &amp; High Temp</td>
<td>p68</td>
<td>21mV</td>
<td>21mV</td>
</tr>
<tr>
<td></td>
<td>p70</td>
<td>22mV</td>
<td>23mV</td>
</tr>
</tbody>
</table>
AC Analysis

- Impedance study using both estimated lumped models lumped and CPM
- Explore different package decap options
- Package decap selection can be made to reduce the peak magnitude of the impedance
- Resonant frequency and peak $|Z|$ depend on the correct Die, Package and PC Board model inclusion

Accurate equivalent die model (C$_{die}$/R$_{die}$) is crucial to obtain the correct resonant peak frequency and $|Z|$
Transient Analysis

- CPM model created for few cycles along with “pre-simulation” initialization
- CPM current profile duration extended by repeating the pattern
- The longer current profile duration allows for PCB simulation initialization
- Comparisons are done to other internal current profile models

Final CPM used has current profile repeated multiple times
36 Bump Voltage Transient Analysis: 0.95VDC, High Temp, Slow Process

CPM, package, PC board power system

Entire simulation time, including initialization

Voltage drop variation at 36 CPM partitions (representing bump locations)
**36 Bump Voltage Transient Analysis:**

1.05VDC, High Temp, Fast Process

**CPM, package, PC board power system**

Entire simulation time, including initialization

**Voltage drop variation at 36 CPM partitions** (representing bump locations)
BGA Pin Voltage Transient Analysis: 0.95VDC, High Temp, Slow Process

CPM, package, PC board power system

Entire simulation time, including initialization

Zoom in to steady state portion

Voltage drop variation at BGA pins
System Power Integrity Analysis

- System power analysis with the CPM die model can predict:
  - Noisy areas in the die
  - Resonance, frequency of resonance, peak $|Z|$
  - Amount of power noise at the bumps
  - Steady state die power noise

- Although a zero to 100% current step can generally not happen in a real world environment, the analysis can help show how other step changes of current can affect the power integrity at the die and at the BGA pins.

- Transient analysis can help to find the best solutions and tradeoffs for die capacitance and package decaps.
System Power Integrity

Limitations

- System Power Analysis depends on accurate, passive and causal models of package, PCB which is difficult to obtain
- Transient analysis with s-parameter can be slow and problematic
- S-parameter models must be accurate from DC to few GHz

Summary

- CPM can accurately predict die behavior for the scenarios under which they are created, but many other operational conditions and modes can exist
- Difficult to correlate system level power integrity with measurements on real boards
- System power integrity simulations can take a long time to complete, depending on the low frequency effects
Q and A