ALPES: Architectural Level Power Planning & Estimation System

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Outline

- Motivation and Problem statement
- Solution with ALPES
- Example Design highlighting some key concepts
- Current Status and Future plans
- Summary

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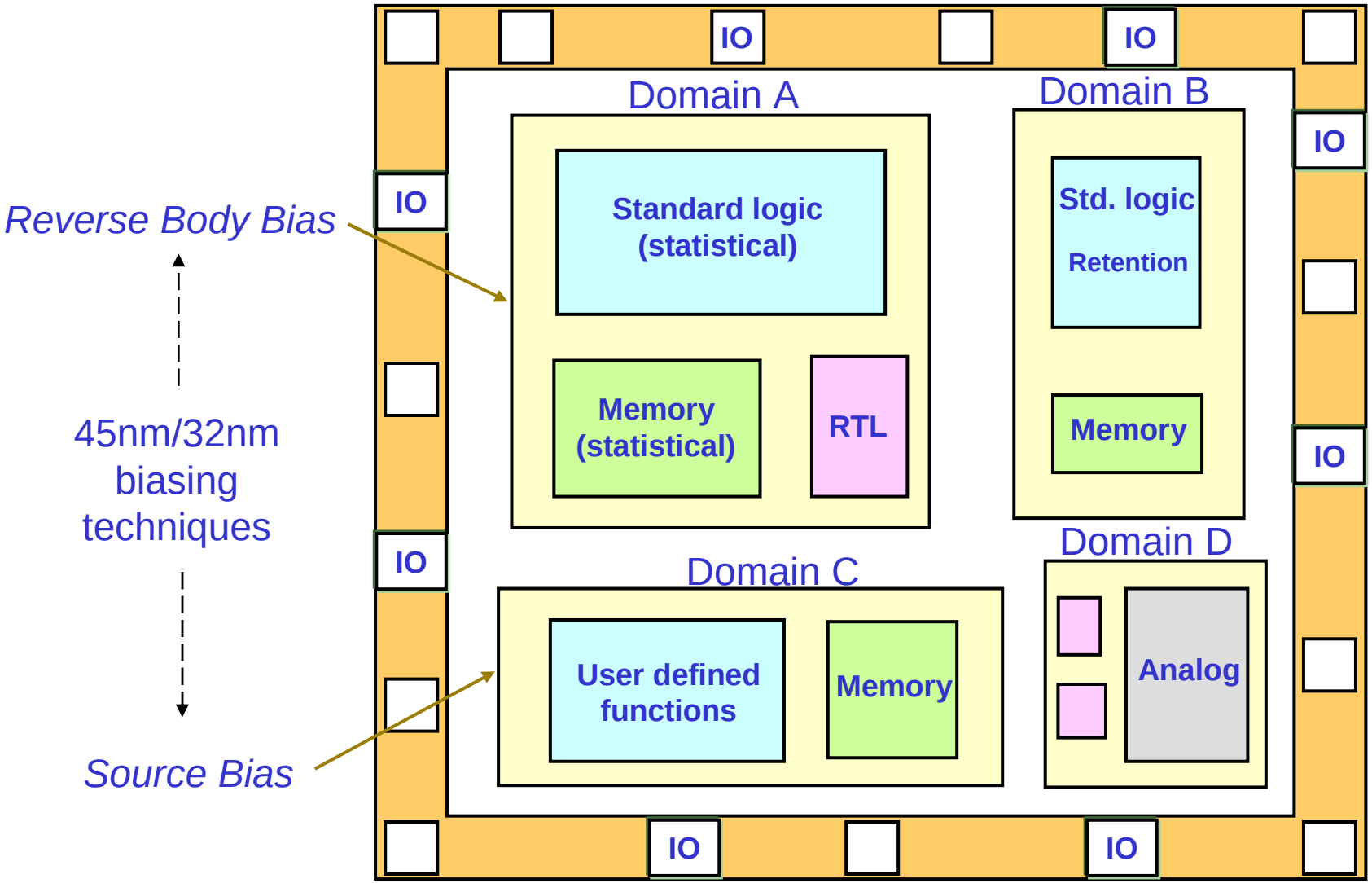
Motivation & Background

- **Power management has become a major concern for Wireless Multimedia applications**
  - *Battery life for mobile phones is a key parameter*
  - *Applications require more and more performances*
- **Reducing Time-to-Market is key in the very competitive Wireless Multimedia market**
- **SoC Low Power Design Complexity is increased**
- **Need EDA tool that maximizes power savings by addressing power consumption at high level of abstraction and by refining it all along design process**

Typical SoC Features/Complexity

- **SOC features**
  - >70 mm²
  - CMOS 45nm and CMOS 32nm
  - >200 Digital/Analog IPs
  - Many µCs, DSPs
  - HW/SW Protocol stacks
  - DDR2-800
  - MBits of SRAM
- **Combination of multiple LP techniques**
  - Dynamic power reduction *(clock gating, DVFS …)*
  - Static power reduction *(power gating, low leakage libraries, retention memories, source biasing, PWM …)*
  - PVT compensation *(reverse & forward body biasing, adaptive voltage scaling, PVT sensors …)*
  - >10 power domains

Comprehensive Power Modeling
Appropriate abstraction of all components



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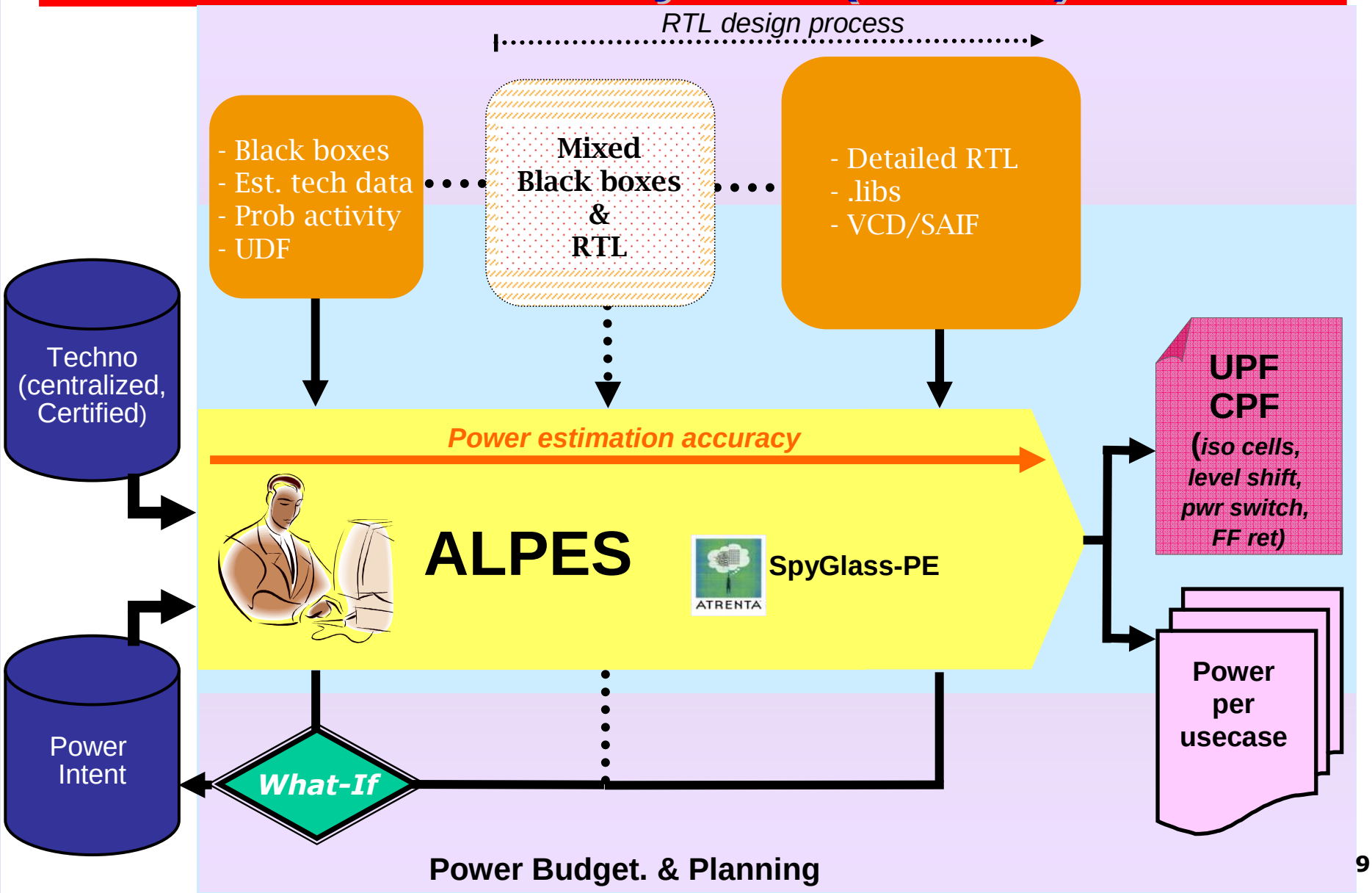
ALPES Solution

- Complex SoC Power is planned at architectural level
- Power Estimation accuracy increases all along the SoC architecture through RTL design process
- Automatic link from architecture to downstream flow (SoC verification & implementation)
- Joint development project with Atrenta

Architectural Level Power Planning & Estimation System (ALPES)



ALPES Technology Inputs

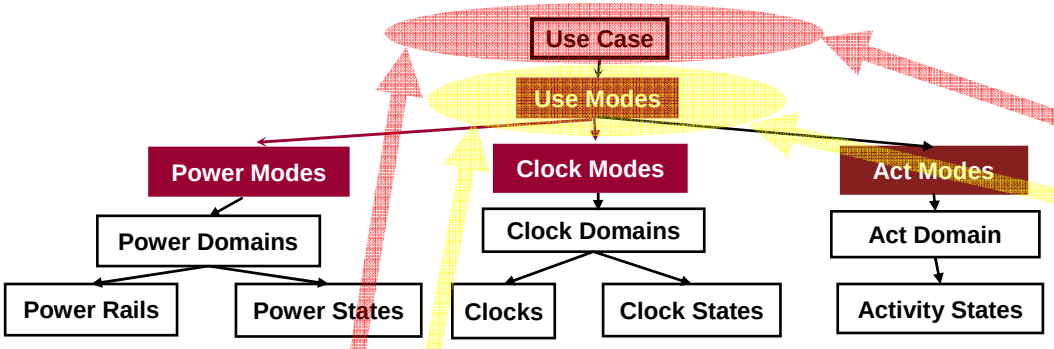
1. **Liberty files**

2. **Certified technology tables**
   - *lots of simulated PVT points per biasing mode*

3. **Central memories database**
   - *To compute memories dynamic power*
   - *To explore memories cuts*

NOTE : (2) & (3) valuable while liberty files are yet to be generated

Scenario Definition



SOC
- SUBS_1_0
  - power_domain_1_
  - power_domain_2_
  - power_domain_3_
- SUBS_2_0
  - power_domain_4_
  - power_domain_5_
- SUBS_3_0
  - power_domain_6_
  - power_domain_7_
  - power_domain_8_
- SUBS_4_0
  - power_domain_9_
  - power_domain_10
  - power_domain_11
- always_on_0

Info | Name | Ports | instances | Connections | Memory_Map | Parameters

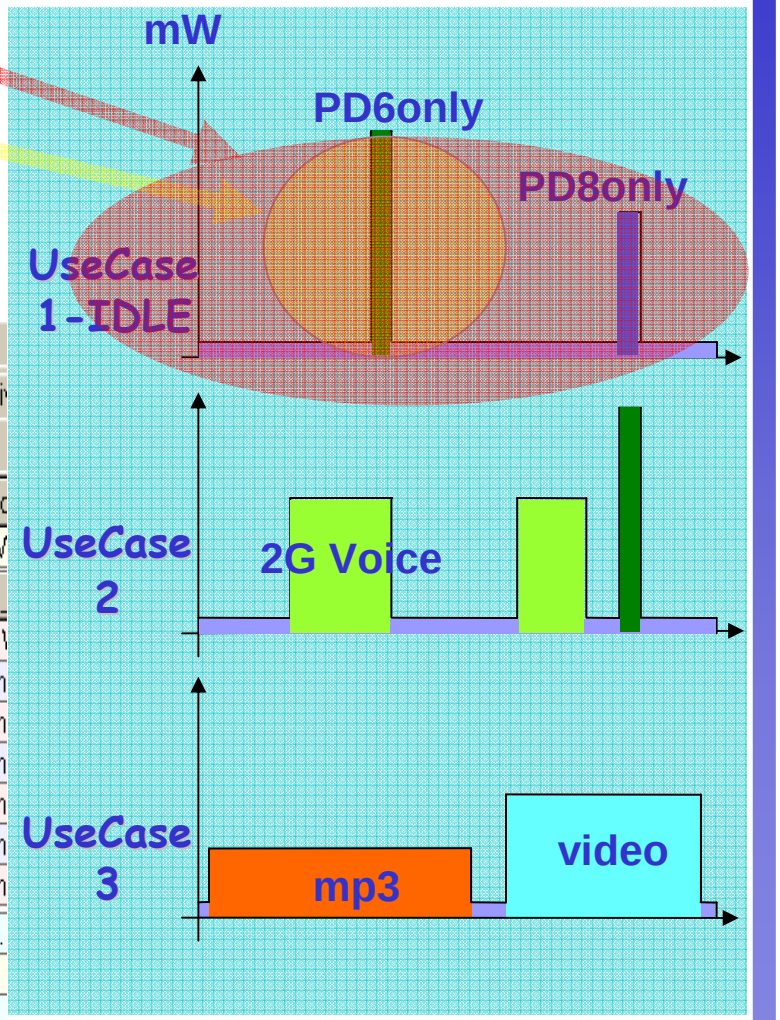
Technology_Info | Technology_Settings | Power | Clocks | Design_Info | Acti

Use_Cases | Use_Mode

	Use_Case	Tem	Power_Es	Leakage_P	Internal_P	Switching_	Total_P
0	USE_CASE1_IDLE	25	Yes	354.11 uW	345.32 uW	2.02 mW	2.72 mW

	Use_Mode	Use_	Leakage_	Internal_Po	Switching_	Total_
0	USE_MODE_PD3_ONLY	0.25	6.40mW	54.9mW	132mW	194m
1	USE_MODE_PD6_ONLY	2.10	1.05mW	4.42mW	11.0mW	16.4m
2	USE_MODE_PD7_ONLY	0	2.84mW	17.7mW	16.7mW	37.2m
3	USE_MODE_PD8_ONLY	2.10	859uW	393uW	4.00mW	5.25m
4	USE_MODE_PD9_ONLY	0.25	2.76mW	42.8mW	21.5mW	67.0m
5	USE_MODE_PD11_ONLY	0	1.12mW	4.26mW	6.35mW	11.7m
6	USE_MODE_AON_ONLY	91.55	318uW	873pW	1.45mW	1.77m

1	USE_CASE1	85	Yes	53.6 mW	54.32 mW	57.74 mW	165.25 ..
2	USE_CASE2_IDLE	25	Yes	388.15 uW	588.31 uW	2.22 mW	3.2 mW
3	USE_CASE2	85	Yes	68.22 mW	71.93 mW	73.05 mW	213.6 ...



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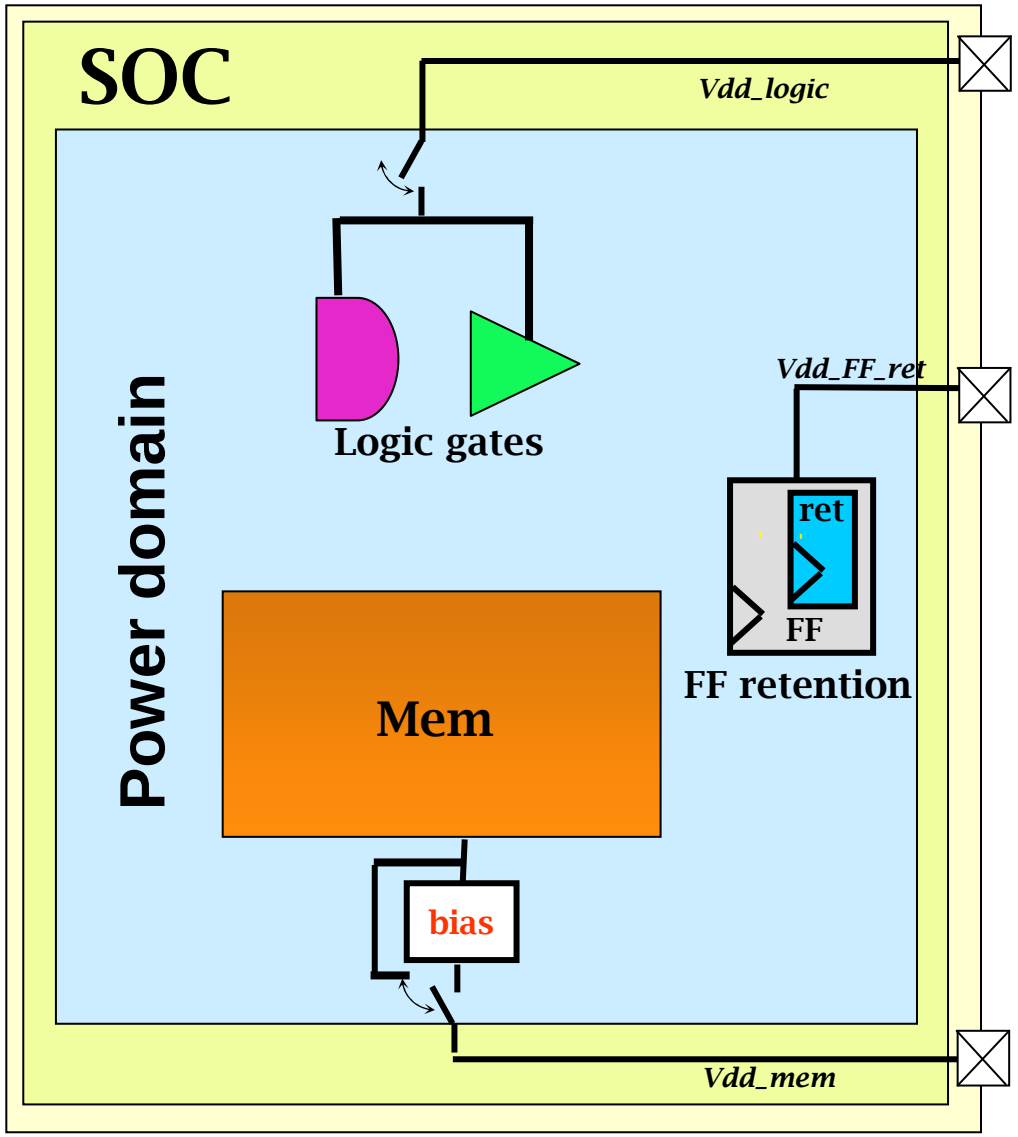
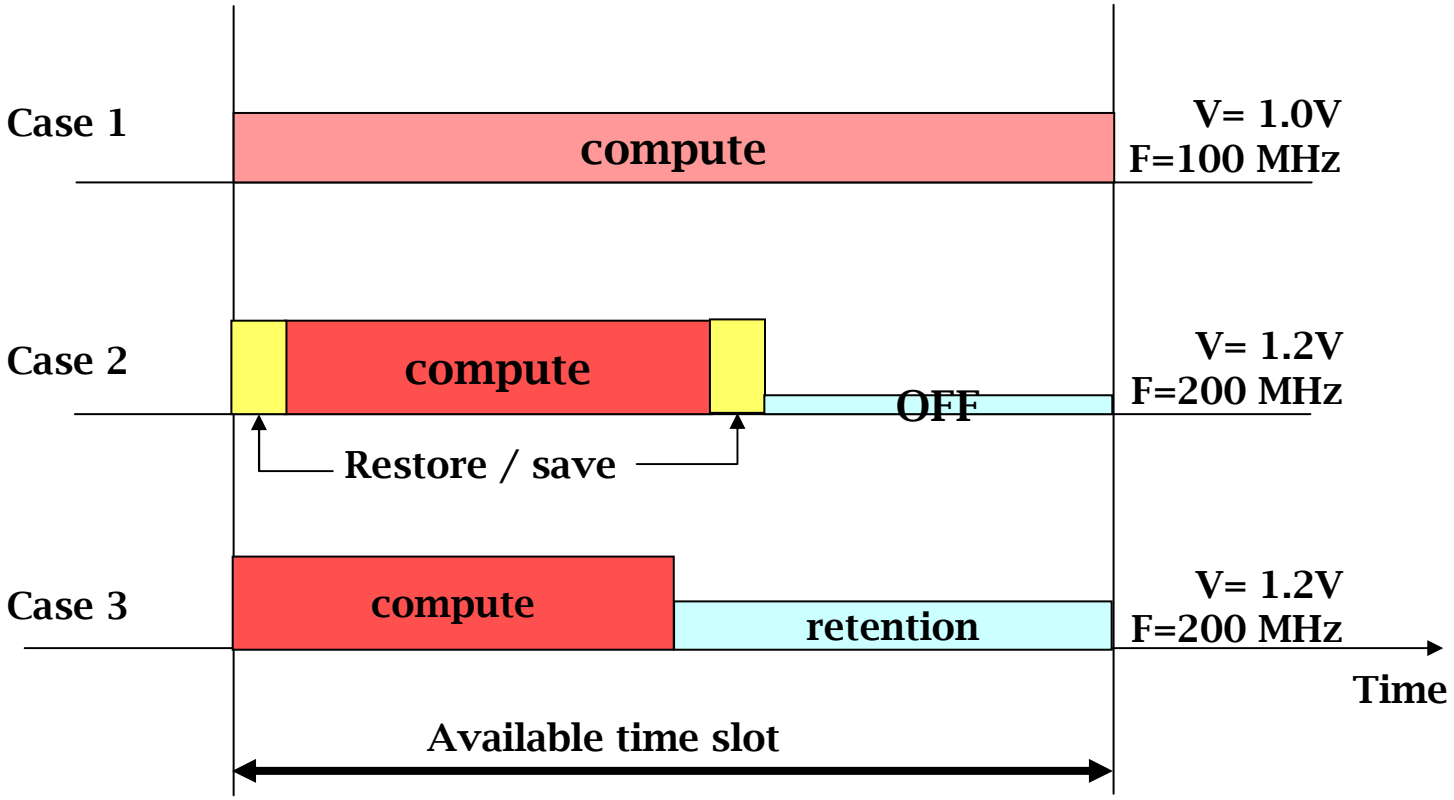
SoC Power Architecture Summary

- DVFS
- Power Switches on logic power rail
- Source Biasing on memories power rail
- FF retention



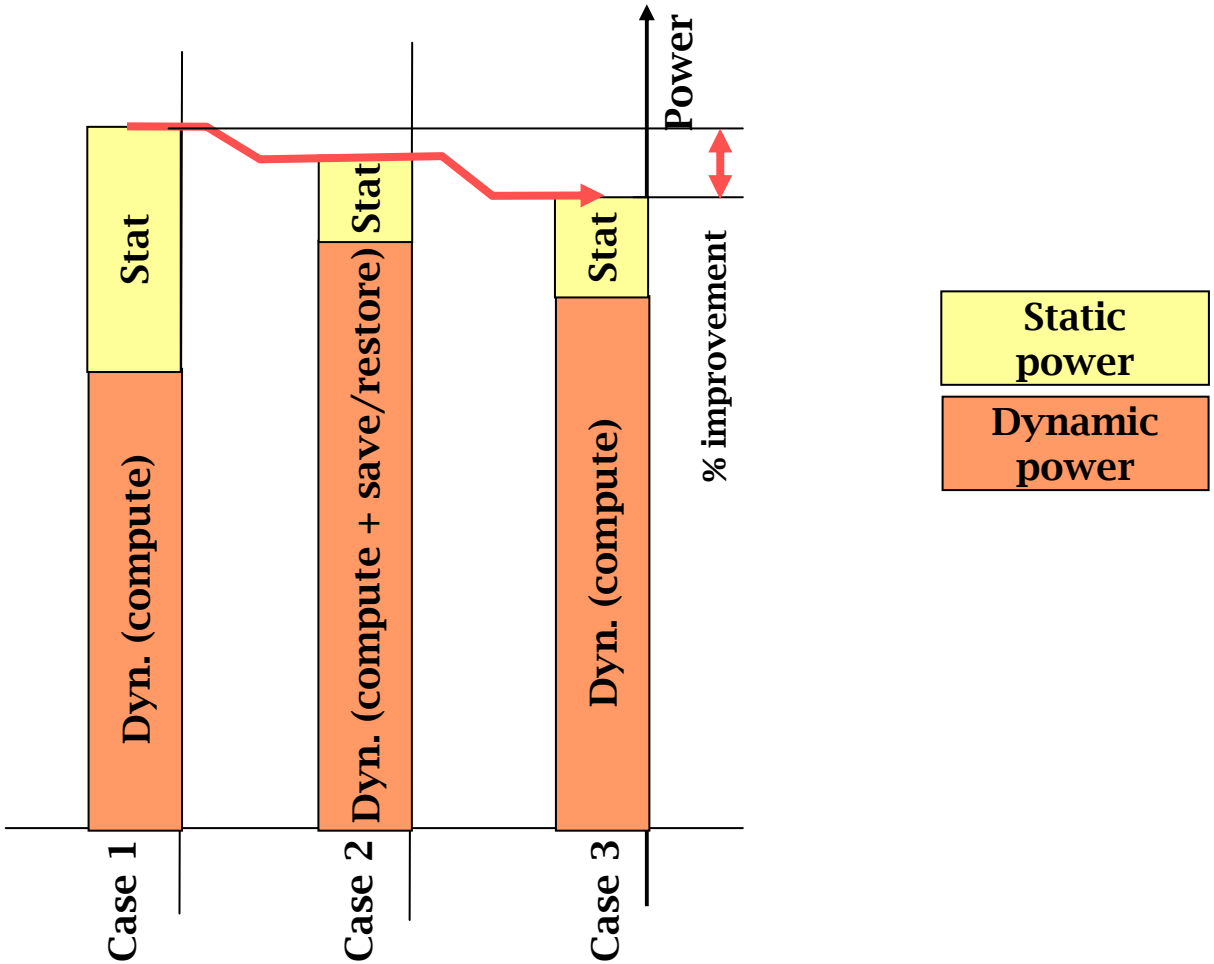
Ex 1 : Power and clock strategy comparison (1/2) (DVFS) - Strategies

- 3 possible strategies for a given computational test case
- Which one to chose?



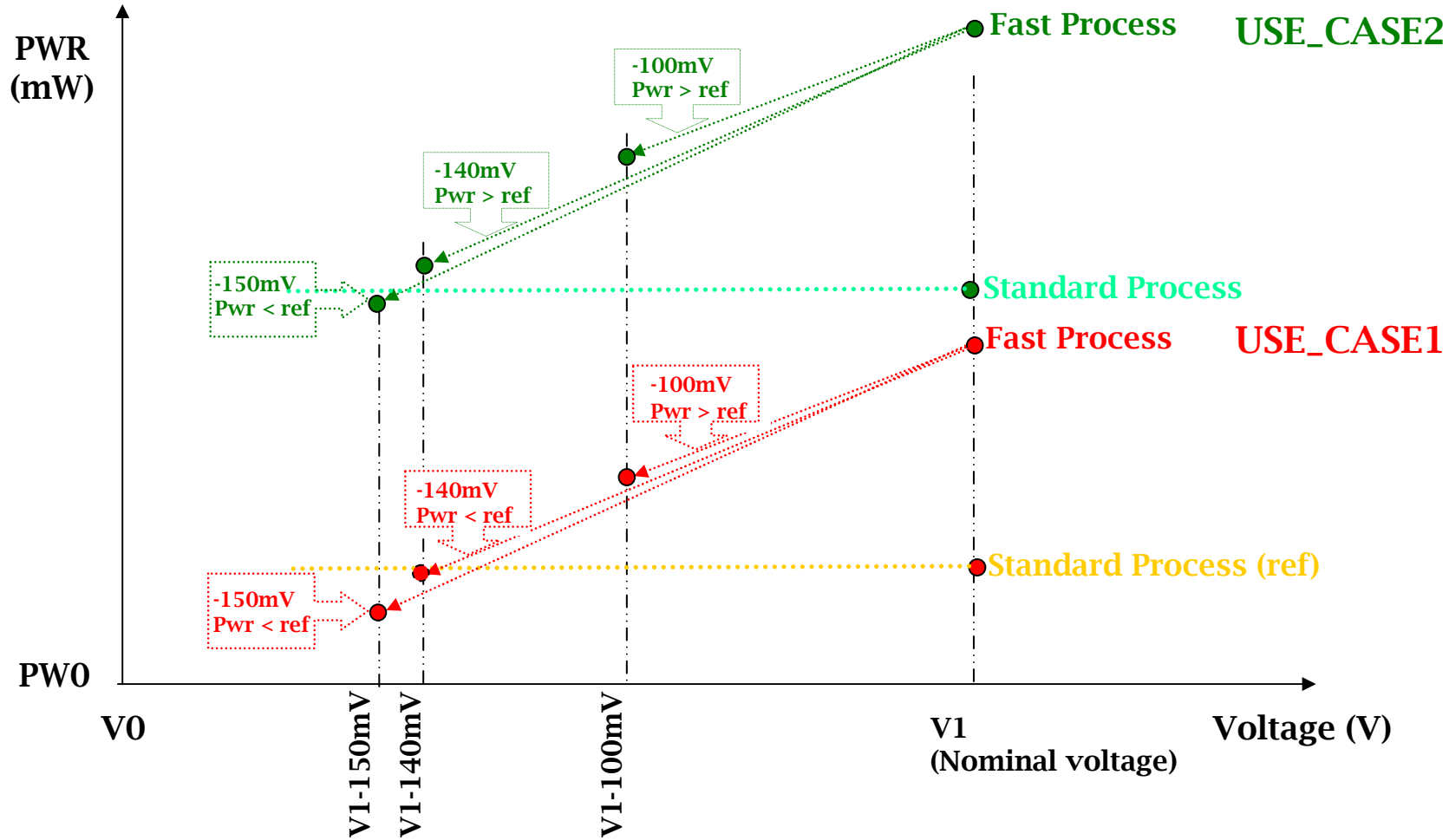
Ex: Power & clock strategy comparison (2/2) (DVFS) – Power consumption results

- Only through Power Estimation we can predict the best approach



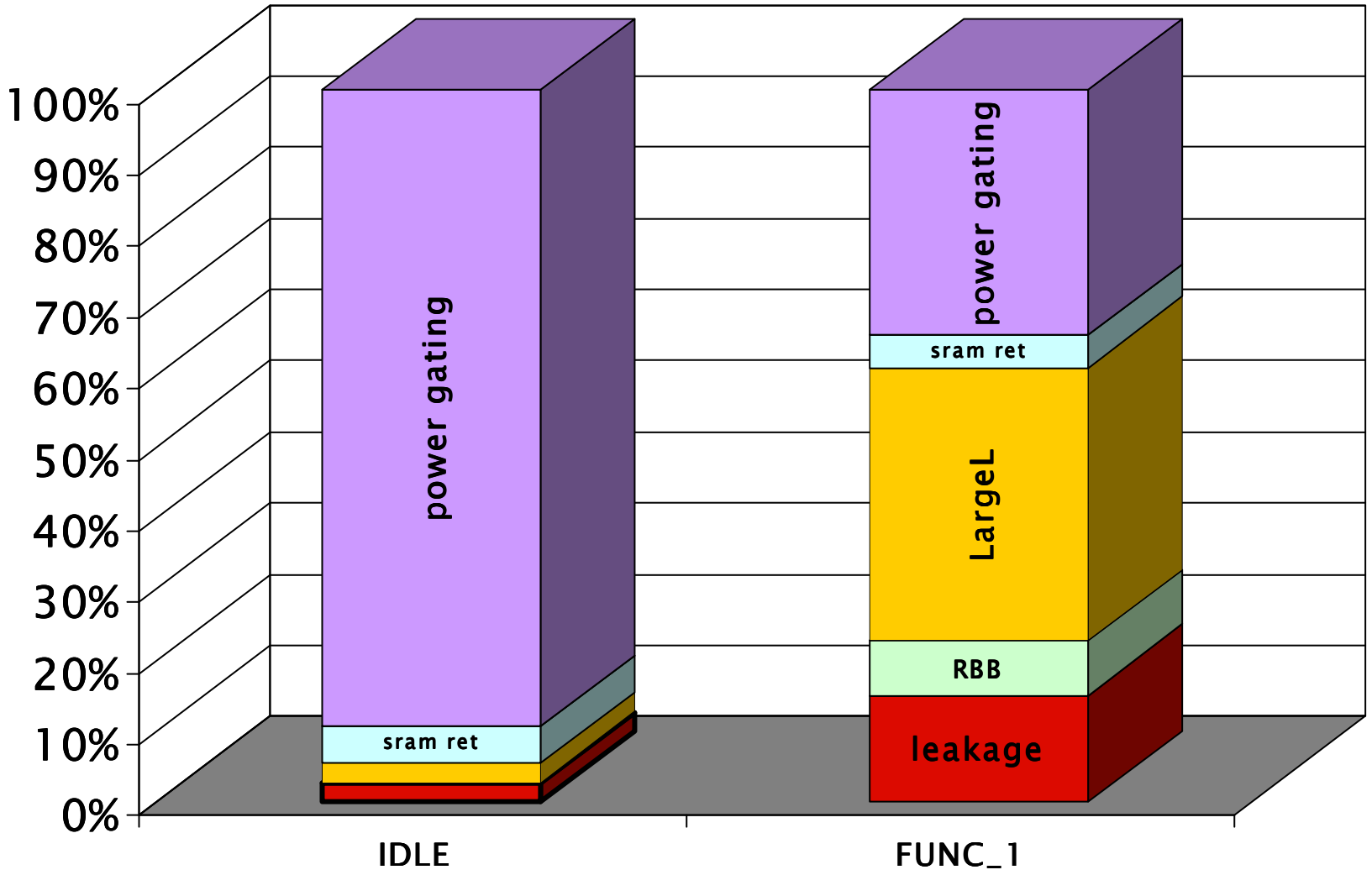
Ex 2 : “What-if” analysis : Voltage scaling

- Voltage reduction to be applied on fast process chips to consume less power than standard process chips



- 150mV voltage scaling has to be applied on fast process chips

Ex 3 : “What-if” analysis : Comparing Leakage Power Reduction Techniques

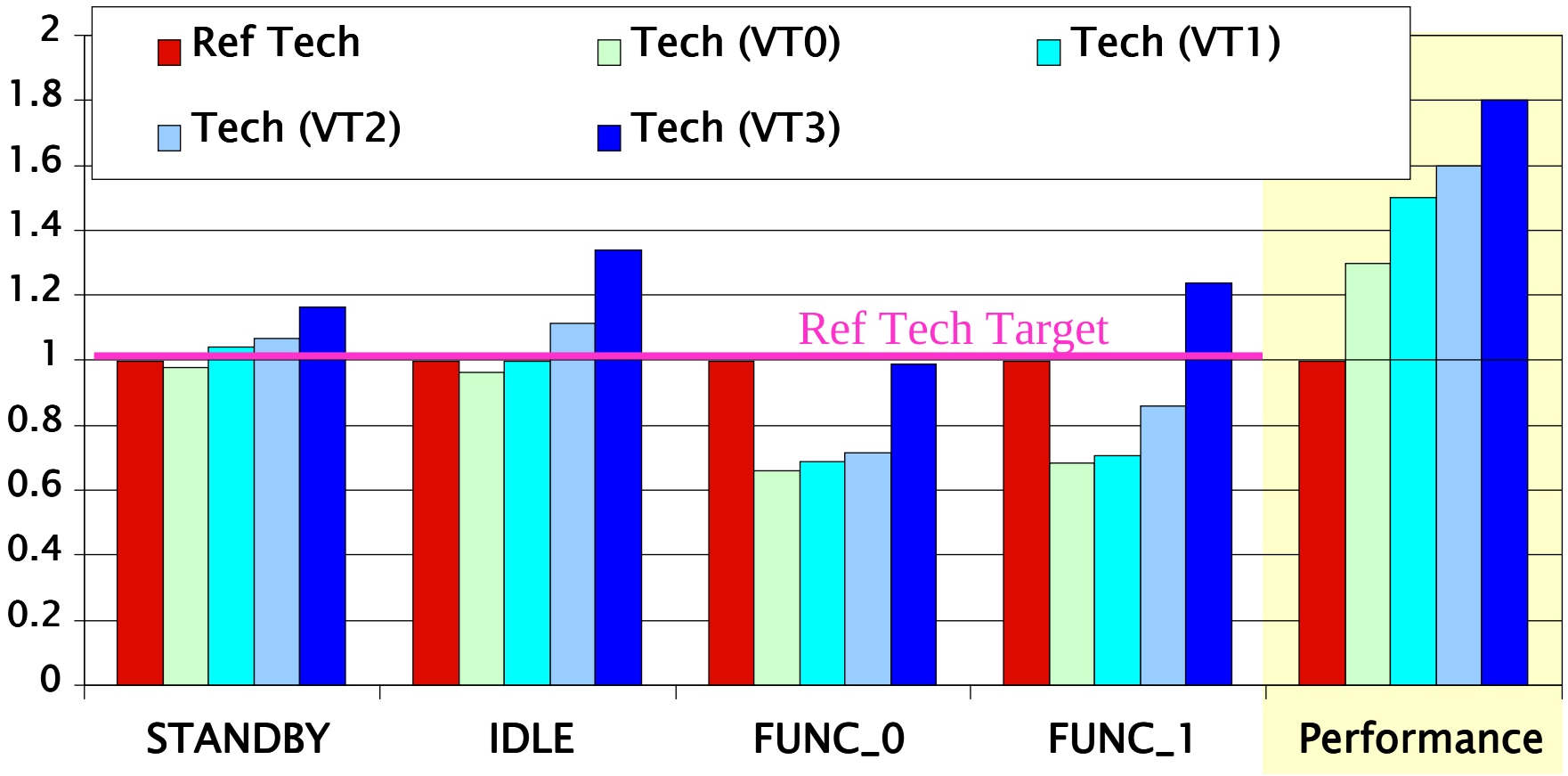


IDLE use case : “power gating” is the key leakage reduction technique.

FUNC_1 use case : “power gating” & “largeL” are key leakage reduction techniques.

ALPES provides powerful what-if analysis for SOC Power Intent exploration

Ex 4 : “What-if” analysis for Voltage Threshold Library selection



Techno brings Power Reduction for all Functional operating modes for (VT0/VT1/VT2)
VT0 required to maintain leakage power (Standby/Idle modes) versus referenced technology

ALPES provides powerful “what-if” analysis for Technology exploration

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Current Status and Future Plans

- Tools utilized in joint development project with Atrenta:
  - SpyGlass® for RTL analysis
  - 1Team®-Genesis for ALPES infrastructure

- Enhancements under consideration:
  - Additional what-if/sensitivity analyses
  - Area modeling
  - 3-D interconnect modeling

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- ALPES tested on large Wireless Multimedia SoC
- Fast power estimation for standard “cell phone” use cases
- Convenient what-if analysis used to experiment power architecture
- Convenient link to downstream flow