

Interconnect Explorer: A High-level Power Estimation Tool for On-Chip Interconnects

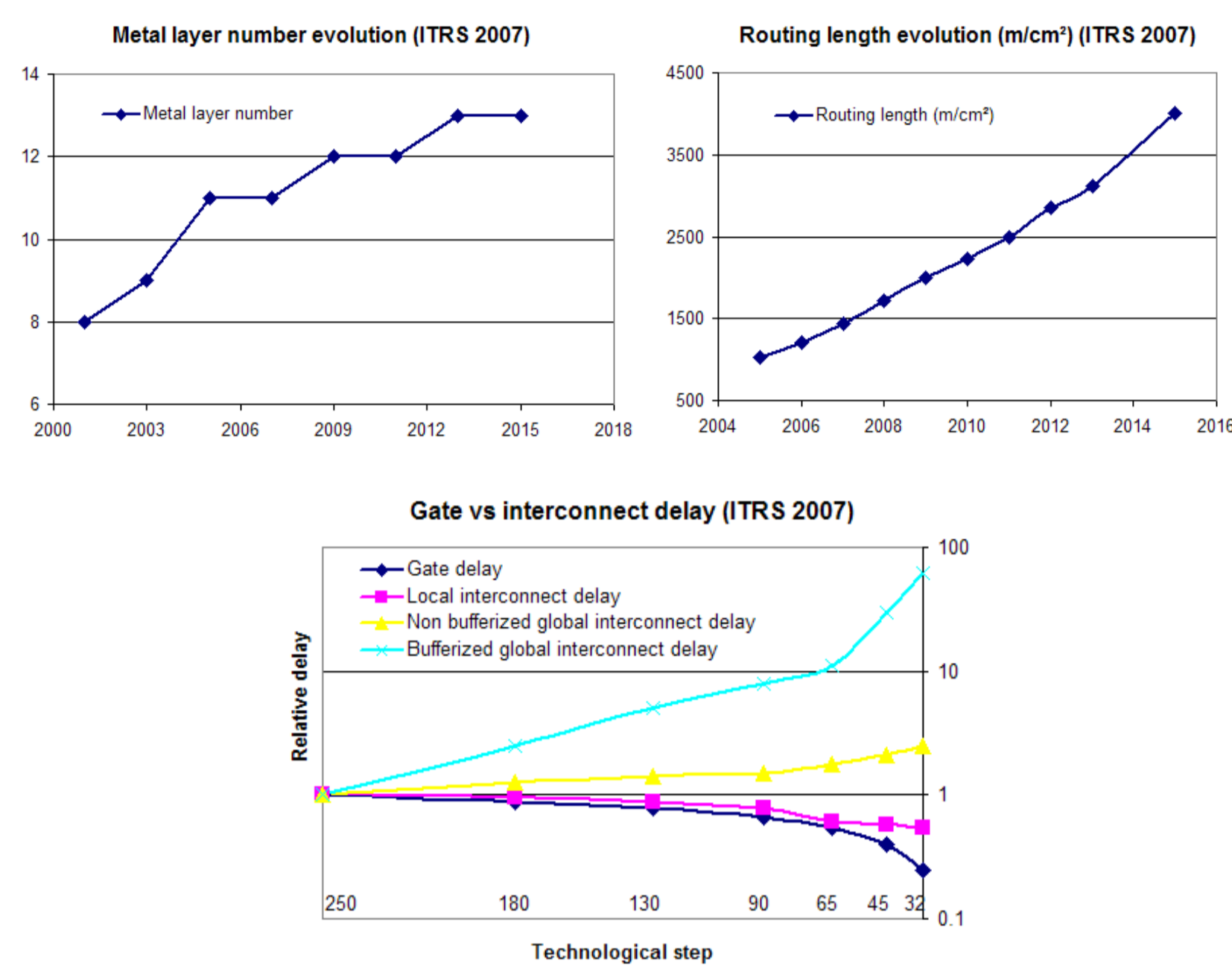
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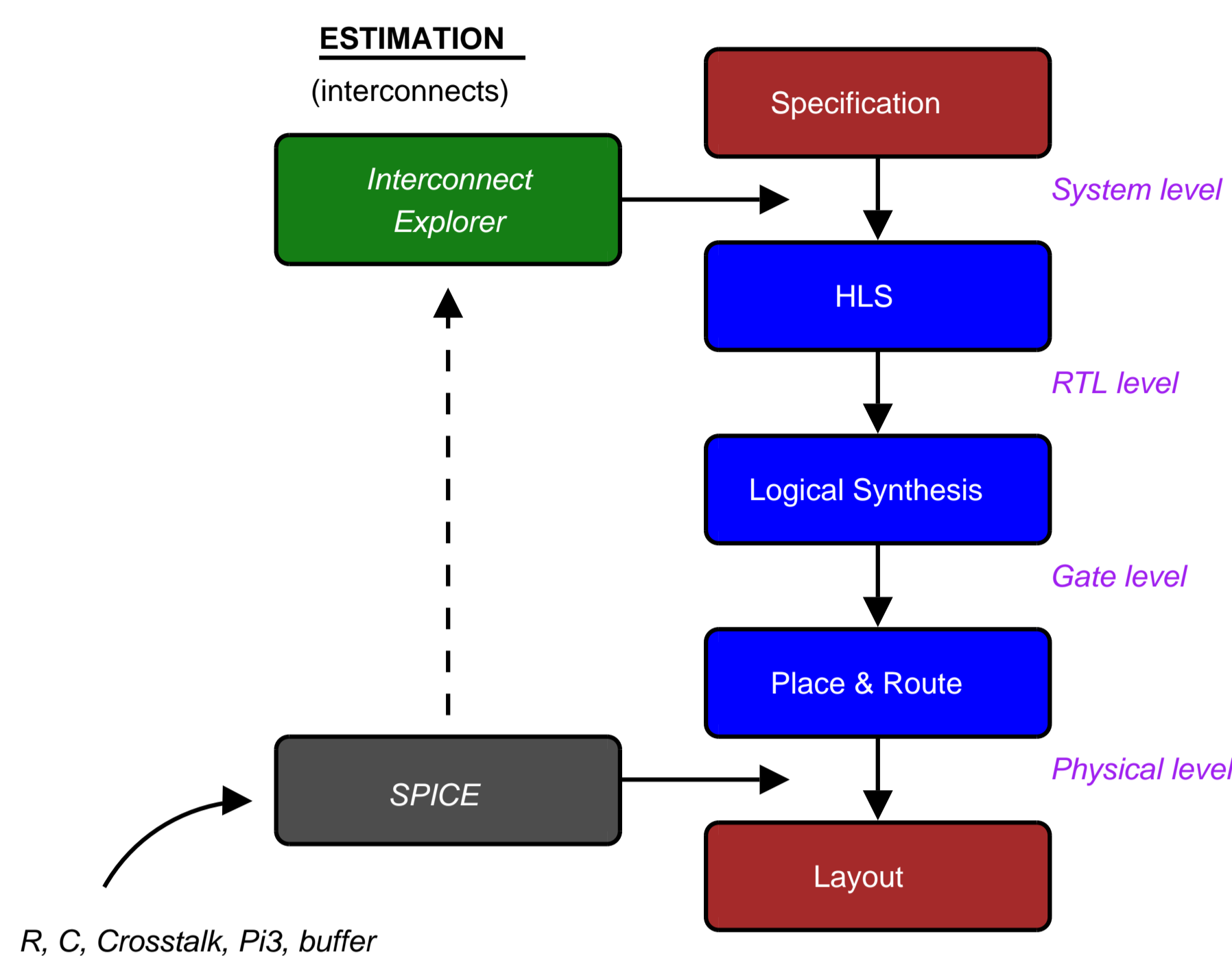
firstname.lastname@univ-ubs.fr – lastname@irisa.fr

CONTEXT



- Interconnect delay > Gate delay
 - Interconnect power consumption around 50% of the total chip power consumption
- ⇒ High-level power estimation tools are needed
 ⇒ Power consumption optimization techniques are needed

DESIGN PROCESS



R, C, Crosstalk, PI3, buffer

PHYSICAL BUS MODELING

Design Kit Values

... LAYER MET2
 TYPE ROUTING
 DIRECTION HORIZONTAL
 PITCH 0.48
 WIDTH 0.20

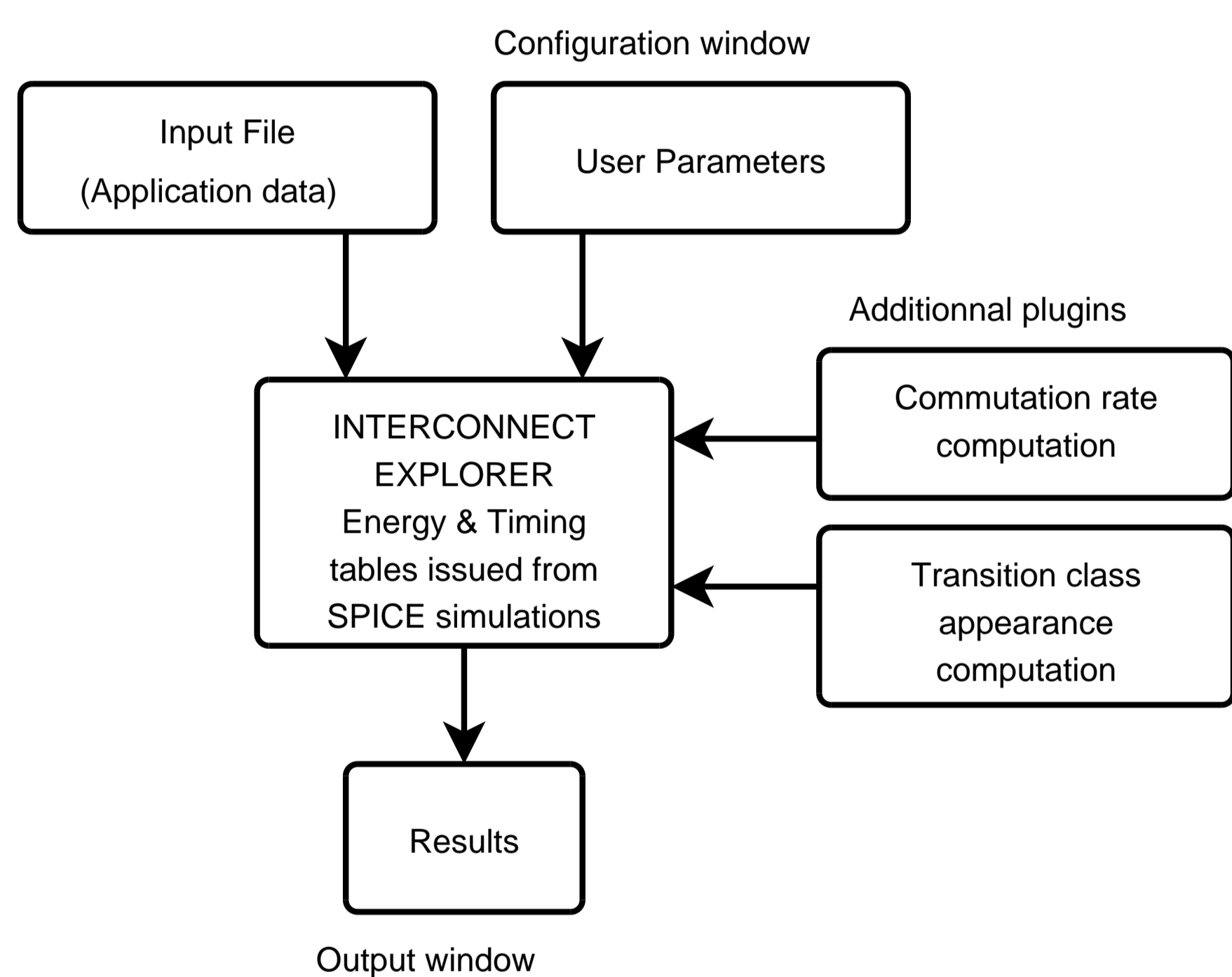
SPACING 0.20
 HEIGHT 1.395
 THICKNESS 0.32
 END MET2

SPICE netlists

```

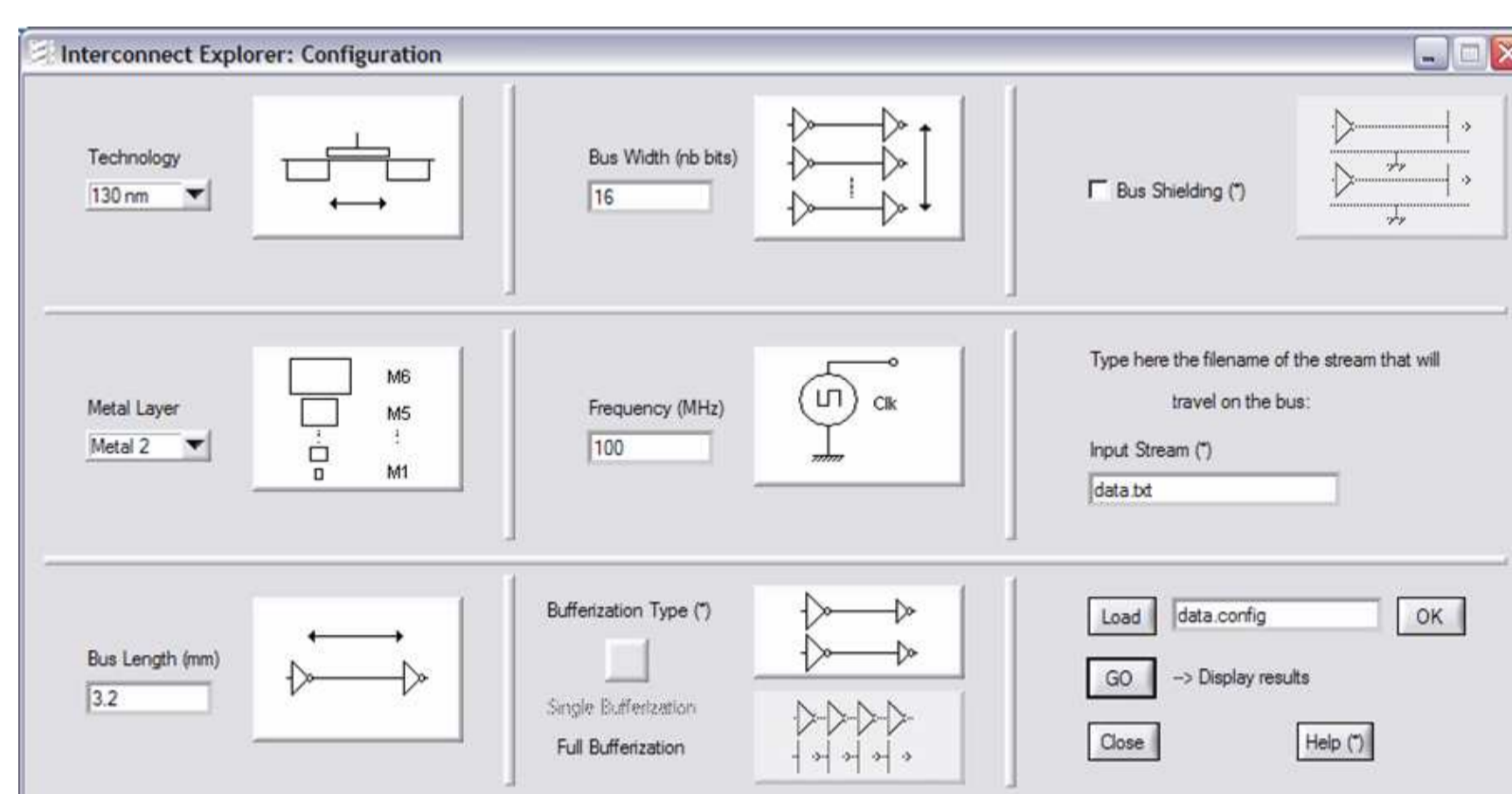
Vin-A1 A10 0 pwl (0n 1.2 0.08n 0.0)
X-invA11 A1 0 A10 A11 inv-str1
X-A1-1 0 A11 A12 Ligne1mm
X-invA12 A1 0 A12 A13 inv-str1
...
CparA11 XA11.In-A XA21.In-A 2.10e-15
CparA12 XA11.N-A1 XA21.N-A1 1.05e-15
...
defwvne pVA=(abs((V2))-i(V2))*0.5*1.2
.tran .01n 10n
.extract integ(w(pVA))
.extract TPD (v(A20),v(A23),VTH=0.60)
    
```

INTERCONNECT EXPLORER ESTIMATION FLOW

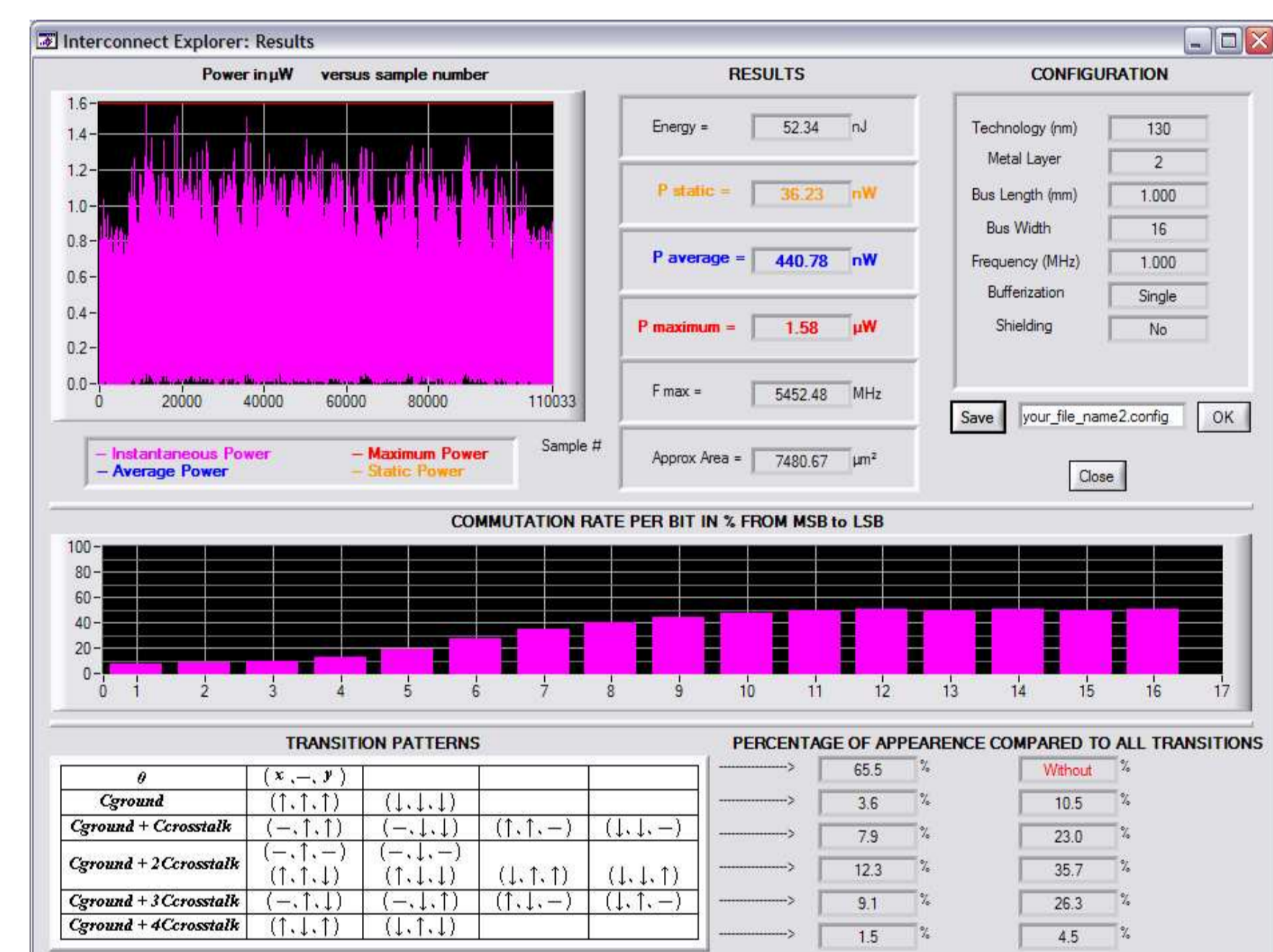


- ⇒ INPUT FILE:
- Application data (image, music, address, instructions ...)
 - Predefined data activity profiles (random, address, image)

INTERCONNECT EXPLORER CONFIGURATION AND RESULTS WINDOWS

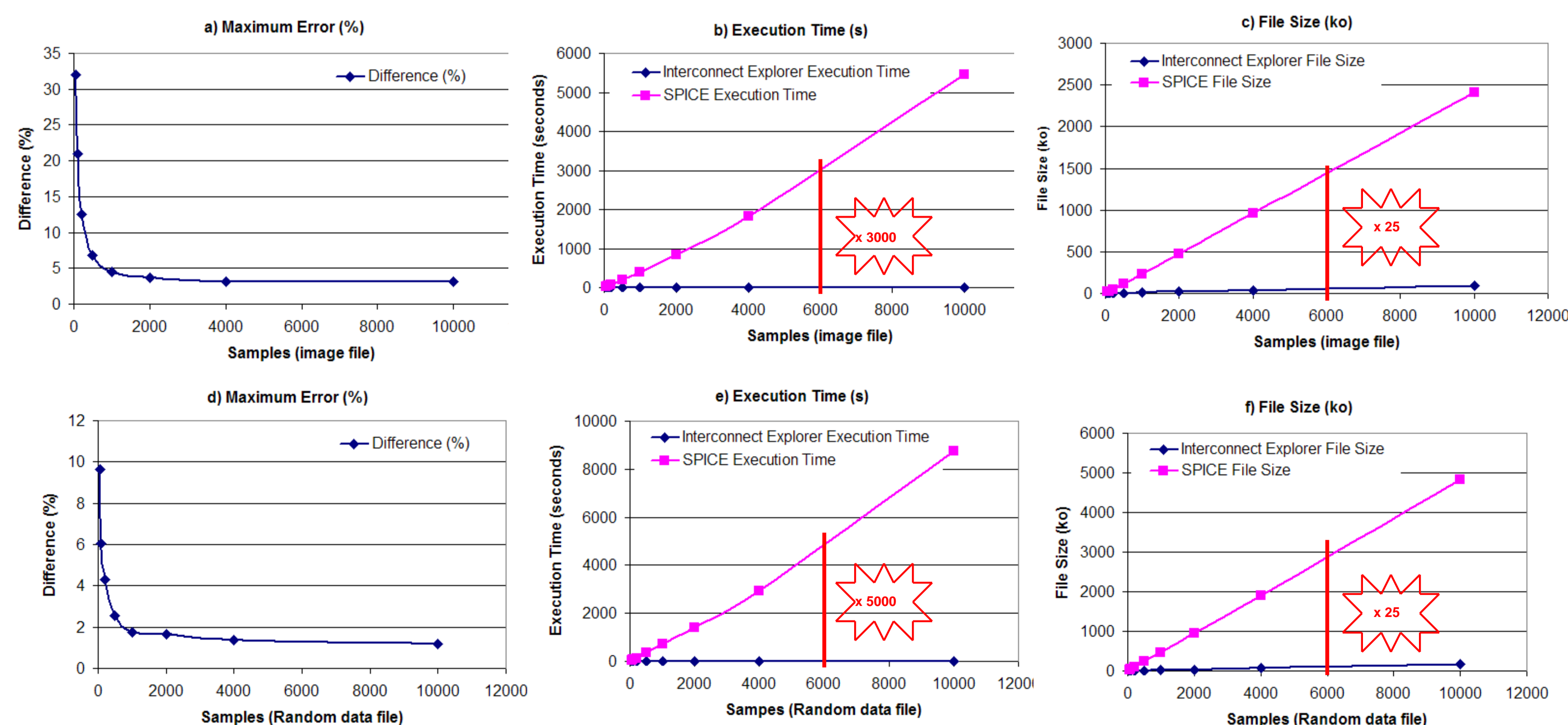


- ⇒ INPUT PARAMETERS:
- Technology
 - Metal layer
 - Bus length
 - Bus width
 - Bus bufferization
 - Bus frequency



- ⇒ OUTPUT PARAMETERS:
- Energy consumption
 - Static, average, instantaneous and maximum power consumption
 - Bus area
 - Bus wire's activity

INTERCONNECT EXPLORER VALIDATION RESULTS



⇒ EXAMPLE: Computing a full HD image energy consumption takes 13 days with the SPICE simulator

FEATURES & BENEFITS

- ⇒ FEATURES:
- High-level estimation tool: *Interconnect Explorer*
 - Fast (few seconds for results computation)
 - Accurate (less than 3% difference with SPICE)
- ⇒ BENEFITS:
- New directions for power optimization
 - Power optimization techniques: *Spatial Switching* & others
 - *Interconnect Explorer* can be used for:
 - MpSOC Approach
 - Mesh, NoC
 - Routing logic consumption
 - MDE (Model Driven Engineering) Approach
 - Platform component based modelization including bus component
 - *Interconnect Explorer* → Plugin for the *OSATE* tool