Soft-error-rate estimation in sequential circuits utilizing a scan ATPG tool

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Background

RAM-ECC in reliable products for automotive and medical use could make logic SER dominant.

Technology Generation

- Logic SER becomes more dominant.
- Estimation of derating effect is important.
Derating Factors for the SER

The following two derating factors alleviate the soft-errors in logic circuits.

Accurate estimation of derating factors is important.

This work

Logical Derating
Masking of error propagation

Timing derating
CLK
input
output
Error signal
not propagating
time
Motivation

The LD estimation of general simulation method is too elaborate, consuming extensive time.
- statistical fault injection (SFI) using gate-level netlists, or using latch-accurate RTL.

This work: a simple but accurate method for LD estimation using a traditional scan ATPG tool.

Analytical Estimation: \( LD = 1 - (1.0 - 0.5)^2 = 0.75 \)

Scan method: \( LD = 1 \)

The propagation probability of AND circuit is 0.5.
The upset data of FFb always affects the FF1 or FF2.
LD Estimation Methodology

It utilizes scan ATPG tool with the scan-test data in the product design flow, and thereby would not require any additional preparation nor input vectors.
# LD Fault Database

V : The fault propagates to some of the next stage FFs
blank : The fault does not propagate to any of the next stage FFs

**Note:** Stuck-at-0 and stuck-at-1 faults are not distinguished.

<table>
<thead>
<tr>
<th>SCAN-IN Random-pattern trial</th>
<th>FF number</th>
<th>Logic derating (LD) = “V” ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 2 3 4 5</td>
<td>for each trial Cumulative for N-trial</td>
</tr>
<tr>
<td>1</td>
<td>V V ..... V</td>
<td>0.254 0.254</td>
</tr>
<tr>
<td>2</td>
<td>V V .....</td>
<td>0.249 0.252</td>
</tr>
<tr>
<td>10000</td>
<td>V V ..... V</td>
<td>0.245 0.252</td>
</tr>
</tbody>
</table>

**LD for each FF**

| 1.00 | 0.05 | 0.01 | 0.13 | 0.85 | ..... | 0.25 |

**Statistically averaged LD:** 0.252
LD Estimation Result

The LDs for each trial are in the range of 22%~28%.

The product microcontroller with approximately 50k FF cells is used for this feasibility study.

The one trial run-time is about 4 seconds.

Logic Derating, LDsingle

Each trial LD
Cumulative LD from trial 1 to trial n

LDsingle ~ 25%
LDsingle:LD at one clock-cycle
LD Distribution for 50k FF

Around 25K out of 50k FFs have the LD less than 5%. Around 10% out of 50k FFs always propagate the injected fault to the next stage.

\[ p \approx 10\% \]

- **No propagated**
- **Always propagated**

Logic derating, LDsingle

Cumulative FF ratio

- 0%
- 25%
- 50%
- 75%
- 100%

p: FF ratio directly coupled to the output

Num. of FFs

0 5000 10000 15000 20000 25000 30000 35000 40000 45000 50000

0-500 1000- 2000- 3000- 4000- 5000- 6000- 7000- 8000- 9000- 10000

Num. of propagated trials out of 10000
Chip LD Estimation

The chip LD (LD<sub>chip</sub>) should be smaller than the LD at one-clock cycle (LD<sub>single</sub>), because the fault reaches to the output after several clock cycles.

<table>
<thead>
<tr>
<th>Num. of CLK to reach output</th>
<th>FF ratio (a)</th>
<th>Logic derating for multi-cycle (b)</th>
<th>contribution (a) X (b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>p</td>
<td>100%</td>
<td>p</td>
</tr>
<tr>
<td>1</td>
<td>(1-p)/3</td>
<td>s</td>
<td>s*(1-p)/3</td>
</tr>
<tr>
<td>2</td>
<td>(1-p)/3</td>
<td>s²</td>
<td>(s²) * (1-p)/3</td>
</tr>
<tr>
<td>3</td>
<td>(1-p)/3</td>
<td>s³</td>
<td>(s³) * (1-p)/3</td>
</tr>
</tbody>
</table>

Total LD<sub>chip</sub> : \[ p + (s + s² + s³)(1-p)/3 \]

p: FF ratio directly coupled to output,
s: propagation ratio from FF to FF at one cycle
Logic Derating for Multi-Clock Cycle

The LD\textsubscript{chip} can be estimated as follows.

\[ LD_{\text{chip}} = p + \left( \sum_{m=1}^{n} s^m \right) \times (1 - p) / n \]

\[ = p + \left\{ s \times (1 - s^n) / (1 - s) \right\} \times (1 - p) / n \ldots (1) \]

The “p” (FF ratio directly coupled to the output) \( \leftrightarrow \) LD distribution results.
The “s” (propagation rate from FF to FF) \( \leftrightarrow \) eq. (2)
The “n” (Average clock-cycle from input to output) \( \leftrightarrow \) FF stage estimation

The LD\textsubscript{single} is equal to that obtained from the scan method.

\[ LD_{\text{single}} = p + s \times (1 - p) = 25\% \ldots \ldots \ldots (2) \]

The “p” is 10% so the “s” is 17%.

\( s \sim 17\% \)
Average Clock Cycle from Inputs to Output

The “n” (average clock cycle from input to output) is around 5.

FF stage MEDIAN=6 → FF-to-FF 5cycle

Ex. 3 stage

n ~ 5
n: average clock cycle from input to output
Logic Derating for Multi-Clock Cycle

The LDchip is estimated to be 12%~13% at n=5.
Summary

- The methodology for simple and accurate SER estimation in sequential circuits including the logic derating was proposed.

- It utilizes scan ATPG tool with the scan-test data in the product design flow, and thereby would not require any additional preparation nor input vectors.

- The LD_{chip} was estimated to be 12%~13% for an embedded-processor.
REFERENCES

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