Semiconductor Pervasion

- Set-Top Box, DVD, Plasma TV, playstation
- Computer, laptops, printers
- PDAs, Digital camera, Cell phones
- Car Multimedia, GPS Tire Pressure Sensor

Semiconductor Market Growth
SOC Power Trends

Power Trend

Power Requirement

Source: IRTS 2005 Power Consumption Trends for Soc-PE
Power Consumption in CMOS

- **Dynamic Dissipation**
  \[ P_{dyn} = C_L \cdot V_{DD}^2 \cdot f_{clk} \]

- **Short-Circuit Currents**
  \[ P_{sc} = I_{sc} \cdot V_{DD} \cdot \left( \frac{t_r + t_f}{2} \right) \cdot f_{clk} \]

- **Static Dissipation**
  \[ P_{stat} = I_{leak} \cdot V_{DD} \]
Scan test vs Functional Power

Functional Mode power consumption

Scan Test Mode power consumption
Power in Scan Test mode

- Power has become the main challenge for nanometer designs.
- Power consumption during test mode is higher (3-8X) as compared to functional mode.
- In low power devices this can increase by 30X !!!
- Such high difference in power consumption can lead to permanent damage.
- Reliability failures due to higher junction temperature and increased peak power.
Power reduction techniques

- Mostly adhoc techniques –
  - Scan chain disabling
  - Scan Segmentation
  - Gating the flop output in shift mode
  - Adjacent fill – Not successful with compression
Low Power Test Methodology

- Low Power Test methodology consists of two stages –
  - Scan insertion
  - Pattern generation
Scan insertion in Low Power designs

- Various industry wide standards like UPF (Unified Power Format) / CPF (Common Power Format) are present for defining the different power domains in the SoC.
- Today, tools have the capability to automatically insert level shifters and isolation cells on scan paths crossing power domains.
- Automated Test control point insertion helps to maintain the required test coverage.
- The level shifter, isolation cell, test control-point insertion is done during scan insertion step.
DFT in Low Power design flow

Synthesis

RTL

UPF /CPF

Test-ready netlist

Logical libraries
(Power attributes)

Multi voltage, OP conditions
ISO cell, level shifter, DRR (Data retention registers)

Scan Insertion

UPF /CPF

DFT-inserted netlist

Physical Implementation

UPF /CPF

DFT-inserted netlist

Physical libraries
(Power attributes)

Power rail, voltage island, Power switch

GDSII
Power distribution analysis

- Design statistics –
  - Division - Automotive
  - Technology 90nm.
  - 1000K design, 50K flops.
  - 8Mhz shift frequency.

![Power distribution chart]

- Shift Mode
  - 14%
  - 33%
  - 22%

- Capture Mode
  - 20%
  - 47%
  - 28%

![Bar chart showing power in mW]
ATPG Capture Power Reduction

Clock gating implementation

- ATPG can control the clock gating logic to clock only those flops that need to switch/store new data.
Low Power ATPG Flow

Estimation of Switching Activity

Generation of Low Power patterns

Validation of generated patterns

Capture Freq

Power Spec

Power Calculation
Vector less Power analysis for diff switching activity (Capture)

Regression Line Plot
Cal the toggling activity

ATPG
set power budget

Low Power patterns

SDF
Full Timing Simulation

VCD

Power Calculation
Dynamic Power analysis (Shift and Capture)

Absolute Power ? Power Spec ?

No

Yes

Done

Refinement of power input to align with Dynamic power analysis
Vectoless Power Estimation

- Power is consumed in - Register, combinational, clock network and black box (memory and IOs).
- Static power estimation tool calculates the power depending upon the switching activity and static probability set for each gate.
- Values are defined for the primary inputs, register and black box outputs.
- For the rest of the design the tool propagated the switching activity and static probability.
Regression Line Plot

- Regression line is plotted to find the curve to best fit the data.
  - Method of least squares.

\[
Slope = \frac{\sum (x - \bar{x})(y - \bar{y})}{\sum (x - \bar{x})^2}
\]

\[
Intercept = \bar{y} - (slope \times \bar{x})
\]
Correlation - vectorless vs absolute

**Clock Power**

- **Capture Power**
- **Shift Power**
- **Vectorless Power**

**Register Power**

**Combinational Power**

**Black Box Power**
Correlation - vectorless vs absolute

![Graph showing correlation between total power and (Flop)Toggling]

- **TOTAL POWER**
- **Power**
- **(Flop)Toggling**

Legend:
- Capture Power
- Shift Power
- Vectorless Power
ATPG Low power pattern generation

- Power aware ATPG can generate low power patterns.
- Need to define the power budget
- Sample script ...

- read the libraries
- read the design netlist
- set the top design
- link
- check clock gating presence
- enable low power engine
- run drc
- set the power budget
- ..
- add faults
- generate atpg patterns
- generate power reports

Enabling low power ATPG

Setting the power budget

Reporting the result
Low power vs std power vectors

Switching activity of Low Power Vs Standard power

- Low Power
- STD_Power
Figures of merit ...

**Capture Power reduction - 20X**

- **Capture Power**
  - Percentage switching
  - Low Power: 1.08
  - STD Power: 22.48

**Test coverage - Same**

- **Test Coverage**
  - Coverage
  - Low Power: 91.66
  - STD Power: 91.63

**Run time increase - 2X**

- **Run Time**
  - Run time (Hrs)
  - Low Power: 36.02
  - STD Power: 18.8

**Pattern Inflation of 2X**

- **Pattern Count**
  - Number of Patterns
  - Low Power: 60784
  - STD Power: 28296
Pattern Validation

- Using Power calculation tool, dynamic power of the generated patterns can be calculated.
- However, due to huge run time and disk space needed for VCD, the step is limited to worst 15-20 patterns only.
- Sample script -
  - read the libraries <worst case for power>
  - read the design netlist
  - set the top design
  - link
  - read the VCD file
  - define the clock ports and clock waveforms
  - define the correct timing window for power analysis
  - report the power
All the patterns have their dynamic power below the power specification of the chip.
Silicon Success ....

- **Application** – Consumer
- **Technology** – 65nm
- **Issue** - ATPG patterns failing due to high power consumption during capture in transition patterns.
- **Number of Transition Patterns** – 36490
- **Number of Scan Cells** – 233850
- **Average Shift Switching** – 46.08%
- **Average Capture Switching** – 7.91%
- **Peak Shift Switching** – 51.08%
- **Peak Capture Switching** – 14.78%
### Shmoo Analysis for std ATPG

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</tbody>
</table>
Low Power Patterns ...

- **Number of Transition Patterns** - 159450
- **Average Shift Switching** - 46.43%
- **Average Capture Switching** - 4.04%
- **Shift Switching** - 51.17%
- **Peak Shift Switching** - 51.17%
- **Peak Capture Switching** - 8.26%
Shmoo for Low Power ATPG

Patterns passed for full functional range!
Conclusion

- Power has become a challenge not only in functional mode but also in test mode.
- The proposed flow, consisting of in-house and EDA tools gives an complete automated flow for low power test methodology.
- The insertion of level shifters, isolation logic and test control point insertion for scan signals is now fully automated.
- Low Power ATPG flow generates low power patterns within the power specification of the design.
Feedbacks to EDA vendors

- Tools should respect the specified power budget value and delete/screen higher switching activity patterns.
- Tools should try to generate patterns close to the specified budget. It will help to reduce pattern inflation.
- The low power pattern inflation is 3-5X. Pattern inflation should be reduced to 2X.
- ‘Filling adjacent bits’ technique is ineffective in reducing shift power in Scan Compression mode.
- Tool should be made capable to write ‘n’ worst power patterns for dynamic power validation.