

Hold Time ECO for hierarchical design

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Agenda

- Introduction
- Contributions
- Hold Time ECO Flow
- Flow Descriptions
- Case Study
- Conceptual Limitations

Introduction

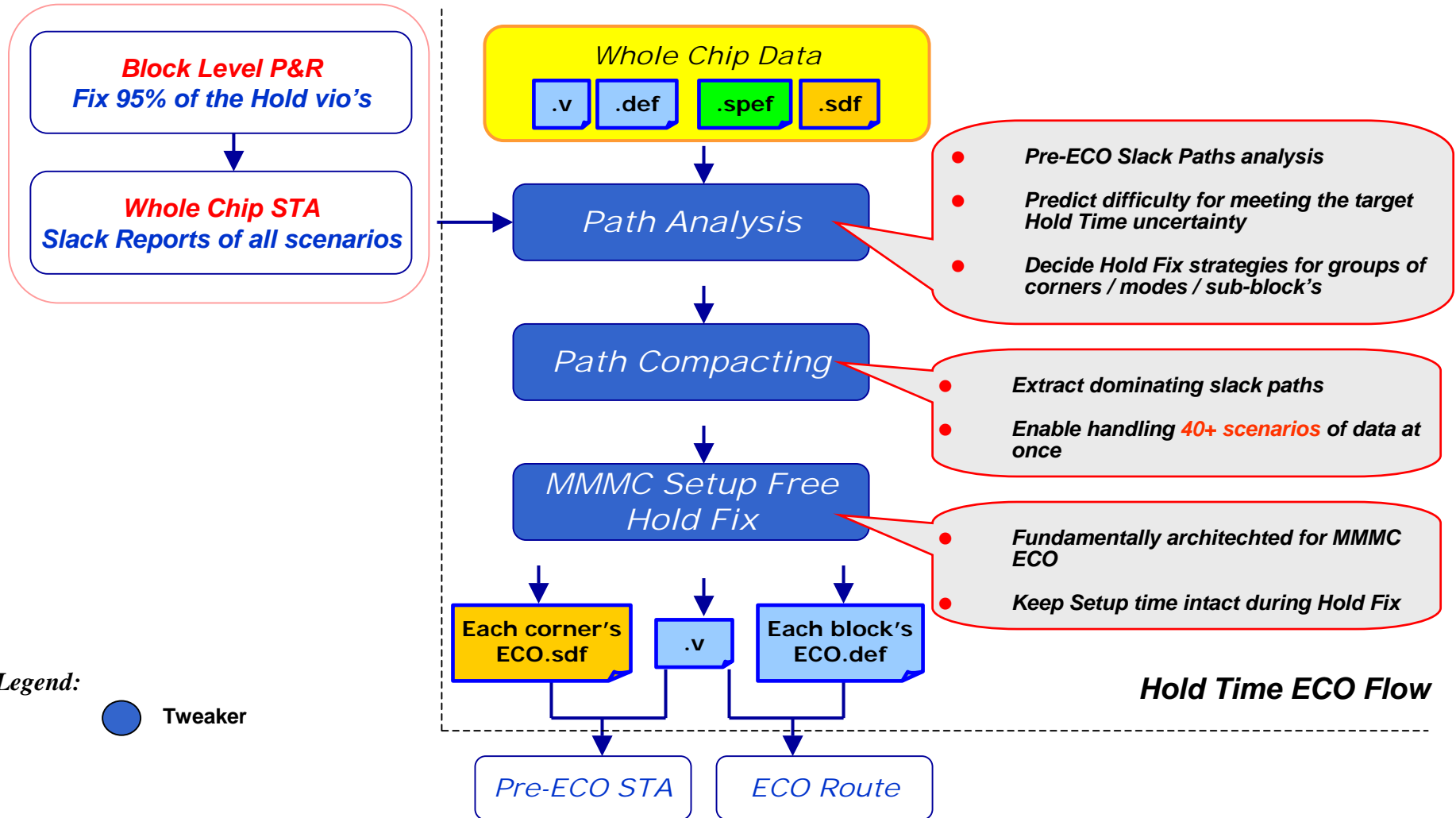
Number of corners, number of modes, and number of sub-design blocks are the three major panic index of today's hold time fixing. The increasing number of corners and modes raises the possibility of cross mode setup-hold conflict, while the increasing number of sub-design blocks results more cross partition timing issues. Either the cross mode or the cross partition timing issues will require large number of ECO's, if not well addressed somewhere else in the design flow.

The hold time ECO flow introduced here dramatically benefits both logic team and physical team with the following major contributions.

Contributions

- Hold time ECO for whole chip at once, not a block by block approach.
 - ⦿ Need only one engineer to handle the ECO job
 - ⦿ Output ECO netlist and ECO placement (DEF) of each block for individual ECO route
- For a real tapeout (65nm/5.2M instances) with eight sub-design blocks, the flow processes 38 STA scenarios at once, within four hours.
- Setup time are kept intact during hold time fixing.
- Pre-ECO analysis validates the targeted hold time uncertainty in advance. It reduces time consuming ECO iterations.
- Flexible hold time fixing strategies for less area overhead.

Hold Time ECO Flow



*MMMC: Multi-Mode, Multi-Corner

Flow Descriptions

Block Level P&R
Fix 95% of the Hold vio's

- Fix 95% of hold time violations at block level P&R
 - ⊙ Assume that the timing will be signed-off based on three RC, four sdc's, and three library corners (36 basic STA scenarios + possible SI/derating scenarios).
 - ⊙ P&R with single RC and sdc's of major operation modes. (Less MMMC scenarios, less loading for P&R tools).
- Leave the last few, say 5%, hold time violations to be addressed by the proposed flow.
 - ⊙ The last few violations can only be fixed by a flow with the capability of handling all scenarios.

Flow Descriptions

Whole Chip STA
Slack Reports of all scenarios

- Dump slack reports of all scenarios at chip level STA.
 - ⦿ The slack reports are of signoff quality. Correlation issues are minimized.
- Feed the slack reports, as well as the signoff SPEF, SDF, and DEF, into the flow.
 - ⦿ The proposed flow is with design data of signoff quality and always take physical information into consideration.

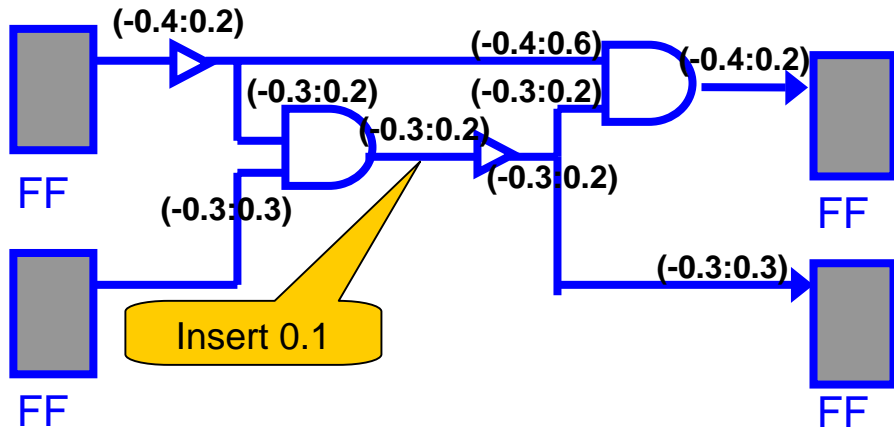
- Pre-ECO slack paths analysis
- Predict difficulty for meeting the target Hold Time uncertainty
 - ⊙ The hold time uncertainty is indeed where the hold time violations come from.
 - ⊙ Effective feasibility prediction reduces time consuming ECO iterations.

- Extract dominating slack paths
 - ⊙ There're many identical paths, with different slack, reside in various scenarios of slack reports.
 - ⊙ By extracting the dominating (unique) paths, the number of Hold Paths fed into the hold time fixing engine can be reduced dramatically.
 - ⊙ Path Compacting enables the flow to handle more than 40 scenarios of slack reports.

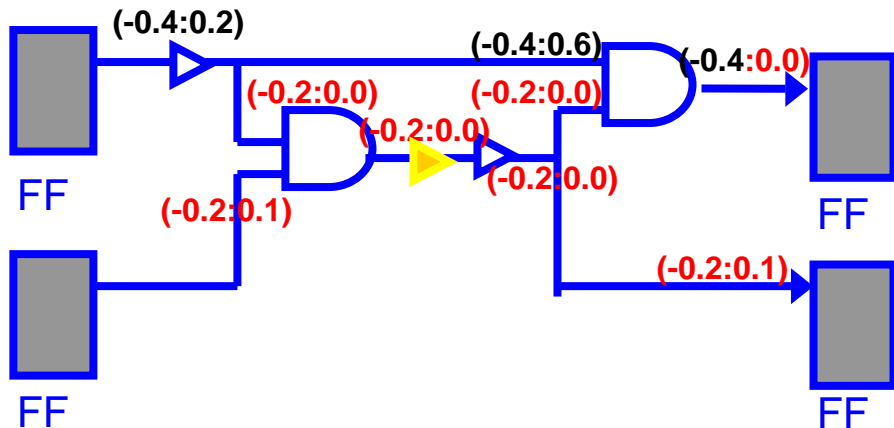
Flow Descriptions

MMMC Setup Free
Hold Fix

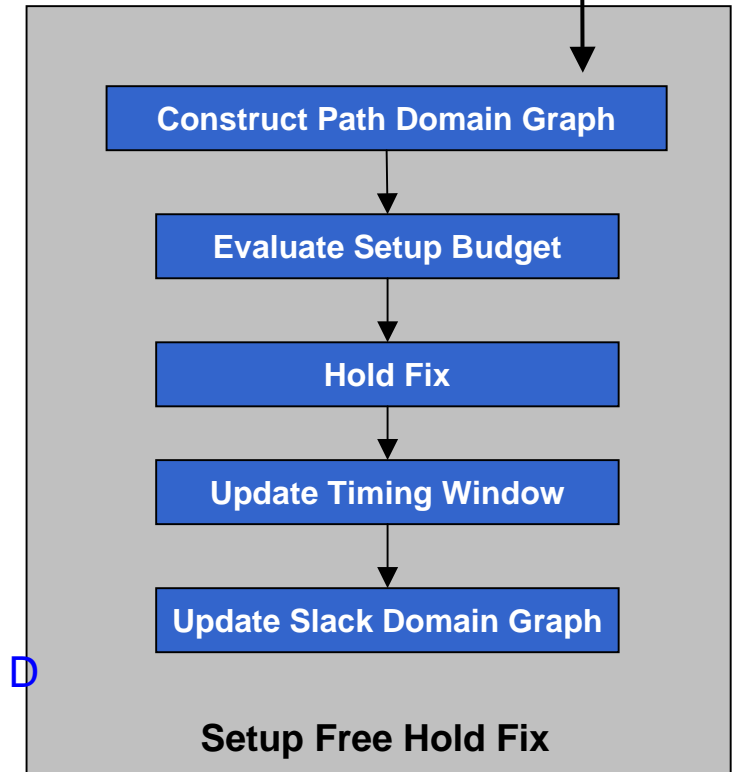
Timing Window Before Buffer Insertion



Timing Window After Buffer Insertion



Merge Timing Window Files
of all scenarios of STA

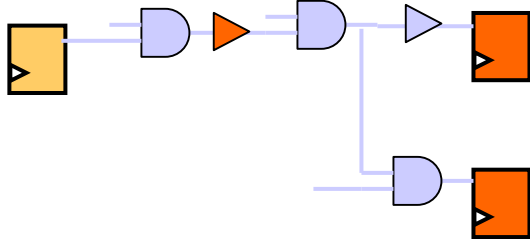


(min slack:max slack) ← pin slack in ns
 fast corner slow corner

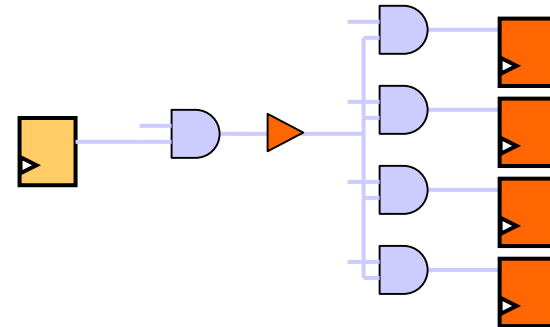
Hold Time fixing strategies

- Various strategies for less area overhead

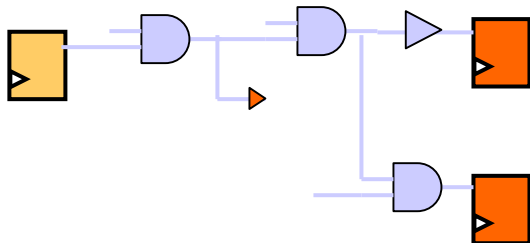
Common Point Insertion



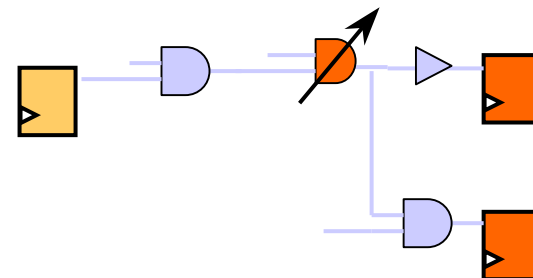
Hi-Fanout Insertion



Dummy Load Hook-up's



Cell Swapping



Case Study

- Design: 65nm / 5.2M instances / 8 sub-design blocks
 - ⊙ Violated Hold Paths: 24362 (end points)
 - ⊙ Number of STA scenarios: 38
 - ⊙ Inserted cells: 11324 cells
 - ⊙ (BUFX1: 9866, BUFX2: 602, BUFX8: 33, DELX1: 823)
 - ⊙ Area: 19740 μm^2 (\approx 140x140)
 - ⊙ Run Time: **4 hours**
 - ⊙ Result: Hold time violations: **24362/-0.70 down to 38/-0.01**
 - ⊙ Setup time violations: **minor impact (could be due to routing change)**

Original		ECO Result	
Setup/WNS	Hold/WNS	Setup/WNS	Hold/WNS
116/-0.3063	24362/-0.70	113/-0.3084	38/-0.01
wc_rctyp_norm	All 38 scenarios	wc_rctyp_norm	All 38 scenarios

Conceptual Limitations

- Run time \propto (number of scenarios x number of hold violations)
 - ⊙ The proposed flow is positioned as a “Hold Time ECO” flow with capability of handling all scenarios of signoff STA. It is not suggested to leave all the hold time violations to be addressed by the flow.
 - ⊙ It is suggest to use your P&R tool to fix 95% of the hold time violations with major but minimum number of scenarios. The idea is simply for relieving MMMC loading of P&R tools but still fully utilize the advantage of P&R tools.