Motivation

Set-Top-Box (STB) SoC designs are extremely complex with multi-million gates, higher core utilization of around 75-80%, and multiple clock domains. Die-Area optimization of such SoCs becomes a key challenge.

Our experience on these SoCs consistently demonstrates that:
- The PDN (Power Delivery Network) lie well within the IVD budget of 15% of supply voltage.
- We continue to see congestion patterns which is shared by both signal/clock due to PG grid overdesign.
- Using an early Power Grid Prototyping based approach, we got results that predicted strong potential for optimizing area of the die without compromising on cost and performance.

In this work, we first leveraged an existing version of the STB SoC and optimized the PDN to (a) quantify the increased signal and routing resources created and (b) its affect on IR drop. In the second phase, we implemented these PDN optimization changes on a shrinkaged version of the SoC and took it through the PnR and timing closure flow to validate the area recovery of these SoCs in production.

Methodology

a) Phase 1- Optimizations using an existing version of SoC:
- Optimize M3 PDN for routing and tracks availability for 7ML and 8ML stack configurations of existing SoC. (M2-M7 stack via for PDN OR M3-M7 stack via)
- Quantify the effect on IR when M7 pitch is made 2x to reduce PG stack vias.

b) Phase 2- Reduced version of SoC (Die area reduced by 12%):
- Took the reduced version of the SoC through PnR, Timing and IR for standard grid (M7 pitch 7.2u) and optimized grid (M7 pitch 14.4u) to validate the Area Recovery.

Results and Findings

Phase 1a: M3 PDN Routability Analysis:

<table>
<thead>
<tr>
<th>Stack</th>
<th>Libs</th>
<th>Grid-A with M3 as supply</th>
<th>Grid-B without M3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Horizontal</td>
<td>Vertical</td>
</tr>
<tr>
<td>7DL</td>
<td>8T</td>
<td>77.1%</td>
<td>90.3%</td>
</tr>
<tr>
<td></td>
<td>12T</td>
<td>84.7%</td>
<td>90.3%</td>
</tr>
<tr>
<td>8ML</td>
<td>8T</td>
<td>77.8%</td>
<td>89.4%</td>
</tr>
<tr>
<td></td>
<td>12T</td>
<td>85.2%</td>
<td>89.4%</td>
</tr>
</tbody>
</table>

Power Grid A allows denser routing for all configurations.

Phase 1b: Optimizing M7 PDN:

The IVD analysis with M7 pitch 7.4u and 14.4u were done using RedHawk-Grid Prototyping System tool, and the worst IR drops were within budgets.

Phase 2: Reduced SoC – Routing Analysis

Routing resources demand at SoC level

Congestion at High Cell Density area

The SoC die-area was reduced while the area of the IP remained the same. This increased routing demands near the Hard IP regions and caused congestions at high-cell density areas.

Summary

- Die-Area optimization of STB SoCs has become a key challenge.
- A two-phase methodology and results for recovering die area of such SoCs in production has been presented.
- In first phase, we leveraged an existing version of the STB SoC and optimized the PDN for 8ML and 8T libraries.
- Our results demonstrate 77% available horizontal tracks with M3 PDN routing versus just 58% without it.
- Also the increase in IR drop is well within the 15% voltage drop budget when the M7 pitch is doubled to reduce the M3-M7 stack via density by 50%.
- In second phase, both the M3 PDN routing and 2x M7 PDN pitch are implemented on a reduced-area version of the same chip and taken through PnR, timing and IR flow to demonstrate the feasibility of recovering the area of the SoC without compromising on performance.