<table>
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<tr>
<th>State-of-the-Art Architectural Exploration for ESL</th>
<th>Space Codesign’s technology brings together state-of-the-art features including electronic system design and simulation, architecture selection, component partitioning and mapping, debugging, monitoring and system generation into a single development environment. Introducing Space Codesign’s ESL solutions into your design process reduces development costs, turnaround time and uncertainties as the system is integrated.</th>
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<td>Get the most from Electronic System Level</td>
<td>For ESL designs, exploration is facilitated and automated, so you can spend more of your valuable design time on your application rather than on architecture considerations. Higher levels of abstraction enhance simulation speed, allowing you to rapidly validate your specifications. Architecture components are simulated to quickly analyze behaviors while taking into account accuracy concerns.</td>
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<td>SystemC made easy for Hardware/Software codesign</td>
<td>Space Codesign’s technology handles the complexity of the SystemC language (IEEE 1666). It brings a unified programming language for hardware and software designs, which significantly reduces the effort required for system integration, hardware/software debugging and system description. Space Codesign also supports TLM-2.0 for improved interoperability.</td>
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<td>Space Codesign™ SpaceStudio</td>
<td>SpaceStudio is our Eclipse-based development environment for the creation, simulation and monitoring of parameterized electronic embedded systems, for system-on-chip. Browse through our SpaceLib components to create your system or insert your own C/C++ design blocks. System configuration and parameters are centralized for easy access. <strong>Architectural exploration through mouse clicks and, drag’n drop</strong> Architectural exploration allows you to quickly discover different system configurations (e.g. number of accelerators and buses, code mapping on hardware or software, hardware coprocessors, etc.) often more than can be considered at Register Transfer Level (RTL), because the work required to experiment with more than a few possibilities was enormous. With SpaceStudio, just drag your application blocks into a hardware-software architecture that you create. A few mouse clicks plus drag-and-drop and voilà! SpaceStudio integrates debugging and monitoring tools, to maximize programmers’ efficiency. Our Elix functional-level ESL technology allows you to validate your specifications by creating SystemC executable models.</td>
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**According to Gary Smith EDA, Space Studio tool suite can be classified as part of the “architect's workbench” category, one of two “killer apps” for ESL and one of the most important.**

**Embedded products**

**FPGA for prototype or end product**
Space Codesign™
ELIX Technology for Functional System Creation

Space Codesign’s Elix technology allows you to validate your specifications by creating SystemC executable models. Our technology presents untimed and timed functional simulations and features mechanisms for virtual platform creation and exploration.

Untimed/Timed Functional - Extremely Fast Simulations
High-Level SystemC design involves message passing, shared memory and register-based communications for rapid specification evaluation.
- Validate your specifications quickly;
- Focus your attention on applications requirements rather than implementation details.

Space Codesign™
SIMTEK Technology for HW/SW Architecture Exploration

Space Codesign’s Simtek technology produces a complete system as a virtual platform before you implement it on an FPGA or ASIC. Simtek allows automatic generation of SystemC TLM2 virtual platform at different levels of accuracy (e.g. AT) for faster simulations and results.

Timed Functional for mapping decisions
Our integrated software environment offers real embedded software development on simulated hardware:
- Automatic generation of C/C++ embedded software;
- Instruction accurate simulation;
- Start writing software before hardware is ready;
- Optimize your hardware according to your software development, creating software-based products;
- Different RTOS choices (μC, VxWorks, RTEm, etc.).

Extensive Exploration through System Partitioning
The Space Codesign™ environment offers architecture exploration with automated partitioning support:
- Code blocks can be imported from Elix functional-level;
- Allocation of processors & HW accelerators;
- Configuration of IP parameters;
- Drag and drop from hardware to software or vice versa, from bus to bus or processor to processor without modifying a single line of code;
- Regenerate and relaunch the final system, and monitor the system changes.

Multiprocessor and Multicore support
Space Codesign’s Simtek allows exploring of architectures over multiple bus or processors.
Supports Xilinx MicroBlaze, PowerPC, Gaisler LEON3 (SPARC) and ARM Cortex-A (multicore) processors. OPB, PLB, AHB and AXI busses are supported.

Space Codesign™
GENX Technology to implement system Hardware and Software

Space Codesign’s GenX technology lets you select and generate all the required hardware and software code, configuration files and parameters to download your system design into a Xilinx FPGA.

Create Prototypes in just a few mouse clicks
By simulating and monitoring your specifications with Space Codesign’s Elix and Simtek before implementing an FPGA, you can maximize your productivity as you create a functioning and tested solution. In the end, you will spend less time debugging your solutions directly on the FPGA.

Synthesize software and communications
Exports RTL implementation of Simtek architectural system:
- RTL hardware IPs and glue logic;
- Embedded firmware and software;
- Project and files for downstream tools (currently Xilinx EDK and ISE);
- Support for High Level Synthesis flows (currently Csynthesizer and CatapultC).

Releases
Version 2.1 of Space Studio™ is available. It includes support for Xilinx Spartan and Virtex. Version 2.2 with support for Xilinx Zynq is coming soon.