



9:00 to 10:15

General Session and Keynote Speaker (no badge required)
Design Automation Can Help the Semiconductor Industry Address Its Many Challenges
William J. Spencer
Chairman of the Board, SEMATECH, Inc., Austin, TX
Opening Remarks • Awards • Keynote Address • (Room: Esplanade Ballroom)

Break

BREAK

10:30 to 12:00

Executive Plenary Panel:
Customers, Vendors, and Universities:
Determining the Future of EDA Together
(No badge required) (Room: Esplanade Ballroom)

Lunch

LUNCH 12:00 - 2:00

RM #

Table with 5 columns: RM 102, RM 301, RM 305, RM 304, RM 103. Rows include Session 1-5 with topics like 'Interfaces for Design Reuse', 'Analog and Mixed-Signal Design Tools', etc.

Break

BREAK

4:30 to 6:00

Table with 5 columns: Session 6-10. Topics include 'Control and Data Driven High Level Synthesis', 'Synthesis Flow in Deep Submicron Technologies', etc.

6:00 to 7:00

DAC Cocktail Party at the San Francisco Marriott 6:00PM - 7:00PM (Yerba Buena Ballroom)

Exhibit Hours 10:00AM-6:00PM / Demo Suite Hours 8:00AM-9:00PM

• Design Methods Track is in shaded area.



RM #	RM 102	RM 301	RM 305	RM 304	RM 103
	Session 11	Session 12	Session 13	Session 14	Session 15
8:30 to 10:00	System-Level Power Optimization	Boolean Methods	Extraction and Modeling for Interconnect	Processor Design and Simulation	Panel: How Much Analog Does a Designer Need to Know for Successful Mixed-Signal Design?
Break	BREAK				
	Session 16	Session 17	Session 18	Session 19	Session 20
10:30 to 12:00	Performance Modeling and Characterization for Embedded Systems	Advances in Placement and Partitioning	Parasitic Device Extraction and Interconnect Modeling	Design Optimization for DSP	Panel: User Experience With High Level Formal Verification
Lunch	LUNCH 12:00 - 2:00				
	Session 21	Session 22	Session 23	Session 24	Session 25
2:00 to 4:00	Bridging the Gap Between Simulation and Formal Verification (Tutorials included)	Logic Optimization	Routing for Performance and Crosstalk	Practical Optimization Methodologies for High Performance Design	RF IC Design Methodology (Tutorial included)
Break	BREAK				
	Session 26	Session 27	Session 28	Session 29	Session 30
4:30 to 6:00	Theory and Practice in High Level Synthesis	BDD Approximation Techniques	Interconnect Modeling and Timing Simulation	Low Power Design Using Multiple Thresholds and Supplies	Panel: Technical Challenges of IP and Systems-on-Chip: The ASIC Vendor Perspective
<p>35 Years of DAC Anniversary Party 7:30PM - 10:00PM at the San Francisco Marriott (Yerba Buena Ballroom)</p> <p>Exhibit Hours 10:00AM-6:00PM / Demo Suite Hours 8:00AM-9:00PM</p>					



RM #	RM 102	RM 301	RM 305	RM 304	RM 103
	Session 31	Session 32	Session 33	Session 34	Session 35
8:30 to 10:00	Software Synthesis and Retargetable Compilation	Formal Methods in Functional Verification	Core Test and BIST	Interconnect Analysis and Reliability in Deep Sub-micron	Panel: Design Productivity: How to Measure It, How to Improve It
Break	BREAK				
	Session 36	Session 37	Session 38	Session 39	Session 40
10:30 to 12:00	Timing Analysis	New Techniques in State Space Explorations	Advanced ATPG Techniques	Practical Experience of Functional Verification for Complex ICs	Panel: The EDA Startup Experience: The First Product
12:00 Lunch 2:00	KEYNOTE 1:00 - 1:45 (Lunch Not Included) <i>From POTS to PANS: Transition in the World of Telecommunications for the Late 90s and Beyond.</i> George H. Heilmeier - Chairman Emeritus, Bellcore, Morristown, NJ Gateway Ballroom (no badge is required to attend)				
	Session 41	Session 42	Session 43	Session 44	Session 45
2:00 to 4:00	Fast Functional Simulation (Tutorial included)	Power Estimation and Modeling	Technology Mapping for Programmable Logic	Power Dissipation and Distribution in High Performance Processors	Panel: Challenge in the Test on System-on-a-Chip Era (Tutorial included)
Break	BREAK				
	RM 301	RM 305	RM 304	RM 103	
	Session 46	Session 47	Session 48	Session 49	
4:30 to 6:00	Controller Decomposition for Power and Area Minimization	IP Protection Technologies	Case Studies of New Design Methods	Thirty-Five Years of Design Automation, a Retrospective and a Look-Forward (no badge required)	

Demo Suite Hours 8:00AM-5:00PM

Tutorials will be held at the Moscone Center in the Esplanade Ballrooms 301-306.

8:00 AM - Tutorial Registration Opens (Esplanade Lobby)

12:00 Noon - Lunch

8:30 AM - Continental Breakfast

5:00 PM - Tutorials End

9:00 AM - Tutorials Begin

Tutorial 1**Room 305****Design Validation Techniques**

Organizer: *Gitanjali Swamy* - Boston Advanced Development Labs., Mentor Graphics Corp., Boston, MA

Tutorial 2**Room 302****Design of Complex Mixed-Signal Systems on a Chip**

Organizer: *Ken Kundert* - Cadence Design Systems, Inc., San Jose, CA

Tutorial 3**Room 303****CAD for System Design: Models, Issues, and Some Emerging Tools**

Organizer: *Gaetano Borriello* - Univ. of Washington, Seattle, WA

Tutorial 4**Room 304****Interconnect Analysis in High-Frequency, Sub-Micron, Digital VLSI Design**

Organizer: *Peter Feldmann* - Lucent Technologies Bell Labs., Murray Hill, NJ

Tutorial 5**Room 301****Finding Design Errors and Locating Defects: The Same Detective Story**

Organizer: *Miron Abramovici* - Lucent Technologies Bell Labs., Murray Hill, NJ

Tutorial 6**Room 306****High Performance RTL Coding Styles for Synthesis**

Organizer: *Joseph Pick* - Synopsys, Inc., Bethesda, MD

If you are interested in the following topics please see the related sessions listed below.

Silicon Village

Sessions: 1, 7, 24, 30, 33, 35, 39, 43, 45, 47

System Design and Optimization

Sessions: 3, 4, 10, 11, 14, 16, 19, 31, 33, 39, 45, 46, 48, Tutorial 3

Logic and High Level Synthesis and Optimization

Sessions: 6, 7, 22, 26, 31, 43, 48, Tutorial 6

Synthesis and Optimization Techniques

Sessions: 12, 27, 37

Design Verification

Sessions: 9, 14, 20, 21, 28, 32, 36, 39, 41, Tutorial 1

Test and Validation

Sessions: 2, 33, 38, 45, Tutorial 5

Deep Sub-Micron

Sessions: 5, 7, 13, 18, 23, 28, 34, Tutorial 4

Interconnect

Sessions: 13, 18, 23, 28, 34, Tutorial 4

Physical Design

Sessions: 7, 17, 23

If you are interested in the following topics please see the related sessions listed below.

High-Performance Design Techniques

Sessions: 14, 24, 44

Low-Power Design Techniques

Sessions: 11, 29, 42, 44, 46

Mixed Signal & RF

Sessions: 2, 15, 25, Tutorial 2

Design Reuse & Intellectual Property

Sessions: 1, 30, 33, 47

Collaborative & Distributed Designs

Sessions: 8, 47

Product & Design Management

Sessions: 8, 35, 40

FPGAs

Sessions: 3, 12, 43

DSP, Communications & Consumer Applications

Sessions: 3, 19, 25, 29, 48

Microprocessors

Sessions: 3, 14, 39, 44

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Tuesday, June 16

opening session

9:00 AM
to
10:15 AM

Esplanade
Ballroom

Opening remarks

Basant R. Chawla

General Chair

Randal E. Bryant

Design Tools Co-Chair

Jan M. Rabaey

Design Methods Co-Chair

technical
program

Awards

James Cohoon

ACM Representative

Bing Sheu

Vice President for Conferences IEEE/CAS

10:30 AM
to
12:00 PM

Esplanade
Ballroom

Opening keynote address

William J. Spencer

Chairman of the Board
SEMATECH, Inc., Austin, TX

Executive Plenary Panel: Customers, Vendors, and Universities: Determining the Future of EDA Together

Chair: *Thomas P. Pennino* - Lucent Technologies, Bell Labs., Holmdel, NJ

Organizer: *Mike Murray* - Acuson Corp., Mountain View, CA

Progress in the the EDA industry depends on the cooperative efforts of customers, vendors, and universities. DAC's opening panel brings together leaders from these communities to discuss how EDA can continue to support rapid innovation in the electronics industry. What are the design challenges ahead? What new EDA technologies and working relationships are required for customers and universities to meet these challenges? What do customers want in a vendor? What do vendors want in a customer? How can universities contribute, and what can customers and vendors do in return? Come join us for a lively and thought-provoking session on the issues which will shape the future of EDA.

Panel Members:

Robert Brodersen - Univ. of California, Berkeley, CA

Johan Danneels - Alcatel Microelectronics, Zaventem, Belgium

Aart de Geus - Synopsys, Inc., Mountain View, CA

Jack Harding - Cadence Design Systems, Inc., San Jose, CA

Wally Rhines - Mentor Graphics Corp., Wilsonville, OR

Gadi Singer - Intel Corp., Santa Clara, CA

(No badge required for this session)

All Design Methods Sessions are shaded green.
Two Plenary Panels are shaded dark green.
(Page 13 and 33)

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uesday, June 16

technical
program2:00
to
4:00§ - denotes
best paperAll speakers are
denoted in **bold**S - denotes
short paper
presentation,
15 minutes**SESSION 1**Room: **102****INTERFACES FOR DESIGN REUSE****Chair:** *Gaetano Borriello* - Univ. of Washington, Seattle, WA**Organizers:** *Timothy Kam, Luciano Lavagno*

Effective reuse of pre-designed components is a key issue in system design, and interface design is an essential technology for achieving it. In this session we have a tutorial devoted to the state of the art in asynchronous design and applications, showing that this is no longer black magic, but a methodology supported by analysis and synthesis tools. This is followed by two papers devoted to synchronous interface synthesis, based on specifications of the interfaced protocols as regular expression and on a fixed finite state machine-based architecture respectively.

1.1 Embedded Tutorial: Asynchronous Interface Specification, Analysis and Synthesis**Michael Kishinevsky** - Intel Corp., Hillsboro, OR**Jordi Cortadella** - Univ. Politecnica de Catalunya, Barcelona, Spain**1.2 Automatic Synthesis of Interfaces Between Incompatible Protocols****Roberto Passerone** - Univ. of California, Berkeley, CA**James A. Rowson** - Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA**Alberto L. Sangiovanni-Vincentelli** - Univ. of California, Berkeley, CA**1.3 Automated Composition of Hardware Components****James Smith**, **Giovanni De Micheli** - Stanford Univ., Stanford, CA**SESSION 2**Room: **301****ANALOG AND MIXED-SIGNAL DESIGN TOOLS****Chair:** *Joseph P. Skudlarek* - Analogly, Inc., Beaverton, OR**Organizers:** *Alan Mantooth, Hidetoshi Onodera*

This session spans many different areas of tools for analog and mixed-signal design. The first paper describes a multi-grid method for solving integrated equations that allow one to extract substitute coupling parameters. Next, a paper is presented on phase noise in oscillators. This paper covers both the theory and methods for characterization. The third paper deals with applying adaptive algorithms to analog test - specifically for fault detection. The last paper describes an automated constraint transformation procedure for top-down analog IC design.

2.1 Multilevel Integral Equation Methods for the Extraction of Substrate Coupling Parameters in Mixed-Signal ICs**Mike Chou**, **Jacob K. White** - Massachusetts Inst. of Tech., Cambridge, MA**2.2 Phase Noise in Oscillators: A Unifying Theory and Numerical Methods for Characterisation****Alper Demir** - Bell Labs., Lucent Tech., Murray Hill, NJ**Amit Mehrotra** - Univ. of California, Berkeley, CA
Jaijeet S. Roychowdhury - Bell Labs., Lucent Tech., Murray Hill, NJ**2.3 Efficient Analog Test Methodology Based on Adaptive Algorithms****Luigi Carro**, **Marcelo Negreiros** - Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil**2.4 General AC Constraint Transformation for Analog ICs****Bogdan Arsintescu** - Delft Univ. of Tech., Delft, The Netherlands**Edoardo Charbon**, **Enrico Malavasi**, **Umakanta Choudhury**, **William H. Kao** - Cadence Design Systems, Inc., San Jose, CA



SESSION 3

Room: 305

UNIVERSITY DESIGN CONTEST

Chair: *Mary Jane Irwin* - Penn State Univ., University Park, PA

Organizer: *Jan M. Rabaey*

A first for DAC, this session presents original electronic designs developed at Universities and resulting in operational implementations. The designs span a diversity of application areas including wireless, DSP, microprocessors and multiprocessors and use design methodologies and techniques ranging from custom ICs, to ASICs, to FPGAs, to PCBs.

3.1 Design Methodology Underlying a Single-Chip CMOS 900 MHz Spread-Spectrum Wireless Transceiver

J. Rael, A. Rofougaran, G. Chang, J. Y.-C. Chang, M. Rofougaran, M. Djafari, P.J. Chang, Asad Abidi - Univ. of California, Los Angeles, CA

3.2 A Video Signal Processor for MIMD Multiprocessing

Joerg Hilgenstock, Klaus Herrmann, Jan Otterstedt, Dirk Niggemeyer, Peter Pirsch - Univ. of Hannover, Hannover, Germany

3.3 Realization of a Programmable Parallel DSP for High Performance Image Processing Applications

Jens Peter Wittenburg, Willm Hinrichs, Johannes Kneip, Martin Ohmacht, Mladen Berekovic, Hanno Lieske, Helge Kloos, Peter Pirsch - Univ. of Hannover, Hannover, Germany

3.4S A Multiprocessor DSP System Using PADDI-2

R.A. Sutton, Vason P. Srin, Jan M. Rabaey - Univ. of California, Berkeley, CA

3.5S The Design and Implementation of The Numachine Multiprocessor

Alex Grbic, Stephen Dean Brown, Steve Caranci, Robin Grindley, Mitch R. Gusat, Guy Lemieux, Kelvin Loveless - Univ. of Toronto, Toronto, ON, Canada
Naraig Manjikian - Queen's Univ., Kingston Canada
Sinisa Srblijic - Univ. of Zagreb, Zagreb, Croatia
Michael Stumm, Zvonko Vranesic - Univ. of Toronto, Toronto, ON, Canada
Zeljko Zilic - Lucent Tech., Allentown, PA

SESSION 4

Room: 304

EMBEDDED SYSTEM DESIGN AND EXPLORATION

Chair: *Ivo Bolsens* - IMEC, Leuven, Belgium

Organizers: *James A. Rowson, Anders Forsen*

The first paper discusses successive formal reinforcement of embedded systems, starting from the general purpose language, JAVA. The second paper explains the mapping of abstract data types into an optimal memory architecture and control. The third paper proposes a new algorithm for mapping a specification on a heterogeneous multiprocessor architecture. The last paper discusses control composition of distributed systems.

4.1 Design and Specification of Embedded Systems in Java Using Successive, Formal Refinement

James Shin Young, Josh MacDonald, Michael Shilman, Abdallah Tabbara, Paul Hilfinger, A. Richard Newton - Univ. of California, Berkeley, CA

4.2 Efficient System Exploration and Synthesis of Applications with Dynamic Data Storage and Intensive Data Transfer

Julio Leao da Silva Jr., Chantal Ykman-Couvreur, Miguel Miranda, Kris Croes, Sven Wuytack - IMEC, Leuven, Belgium
Gjalt de Jong - Alcatel Telecom, Antwerpen, Belgium
Francky Catthoor, Diederik Verkest, Paul Six, Hugo De Man - IMEC, Leuven, Belgium

4.3 Design Space Exploration Algorithm for Heterogeneous Multi-Processor Embedded System Design

Ireneusz Karkowski, Henk Corporaal - Delft Univ. of Tech., Delft, The Netherlands

4.4 Modal Processes: Towards Enhanced Retargetability Through Control Composition of Distributed Embedded Systems

Pai Chou, Gaetano Borriello - Univ. of Washington, Seattle, WA

SESSION 5

Room: 103

TAMING NOISE IN DEEP-SUBMICRON DIGITAL DESIGNS

Chair: *Kenneth L. Shepard* - Columbia Univ., New York, NY

Organizers: *Kenneth L. Shepard, Takahide Inoue*

5.1 Embedded Tutorial: Design Methodologies for Noise in Digital Integrated Circuits

Kenneth L. Shepard - Columbia Univ., New York, NY

Panel: Taming Noise in Deep Submicron Digital ICs

Chair: *Nagaraj NS* - Texas Instruments, Dallas, TX

Organizer: *Takahide Inoue* - Sony Corp., Milpitas, CA

As technology scales into the deep submicron regime, noise immunity is becoming a metric of comparable importance to area, timing, and power for the analysis and design of digital VLSI chips. Noise has two deleterious effects on digital design. In the most serious cases, it can produce functional failures in hardware. Even when noise is not severe enough to cause hardware fails, it can have an impact on timing, affecting both delay and slew. This panel will consider the noise issues involved in the design of circuits and interconnect as well as the important trade-offs that exist between noise immunity and performance.

PANEL MEMBERS:

Barbara Chappell - Intel Corp., Hillsboro, OR
John MacDonald - Sun Microsystems, Palo Alto, CA
Bob Masleid - IBM Corp., Austin, TX
John McBride - Hewlett-Packard, Fort Collins, CO
Chris Noughton - Digital Equipment, Hudson, MA
Kenneth L. Shepard - Columbia Univ., New York, NY
Xiaonan Zhang - Metaflow Technologies, Inc., La Jolla, CA

4:30
to
6:00§ - denotes
best paper**SESSION 6**Room: **102****CONTROL AND DATA DRIVEN
HIGH LEVEL SYNTHESIS****Chair:** *Kayhan Kucukcakar* - Motorola, Inc.,
Tempe, AZ**Organizers:** *David Ku, Timothy Kam*

This session contains papers that describe novel advances in the theory and practice of high level synthesis. The first paper describes a transformational approach to control-intensive designs. The second paper incorporates speculative execution in the scheduling of control-flow descriptions. The third paper reformulates synthesis in terms of data transfers, and the last paper describes rate optimal design of recursive dataflow graphs.

**6.1 Fact: A Framework for the Application of
Throughput and Power Optimizing
Transformations to Control-Flow Intensive
Behavioral Descriptions****Ganesh Lakshminarayana, Niraj K. Jha** -
Princeton Univ., Princeton, NJ**6.2 Incorporating Speculative Execution into
Scheduling of Control-Flow Intensive Behavioral
Descriptions****Ganesh Lakshminarayana** - Princeton Univ.,
Princeton, NJ**Anand Raghunathan** - NEC USA, C&C
Research Labs., Princeton, NJ**Niraj K. Jha** - Princeton Univ., Princeton, NJ**6.3S The DT-Model: High-Level Synthesis Using
Data Transfers****Shantanu Tarafdar, Miriam Leeser** -
Northeastern Univ., Boston, MA**6.4S Rate Optimal VLSI Design from Data
Flow Graph****Moonwook Oh, Soonhoi Ha** - Seoul National
Univ., Seoul, Korea**SESSION 7**Room: **301****SYNTHESIS FLOW IN DEEP
SUBMICRON TECHNOLOGIES****Chair:** *Ralph H.J.M. Otten* - Delft Univ. of Tech.,
Delft, The Netherlands**Organizers:** *Sharad Malik, Randal E. Bryant*

This session examines the impact of deep submicron technologies. It starts with an embedded tutorial on possible approaches for dealing with this impact. It is followed by a paper that presents a methodology for combining technology mapping with floorplanning and placement.

**7.1 Embedded Tutorial: Logic Synthesis for
Ultra Deep Sub-Micron (UDSM)****Robert K. Brayton** - Univ. of California,
Berkeley, CA**7.2 A DSM Design Flow: Putting
Floorplanning, Technology-Mapping, and Gate-
Placement Together****Amir H. Salek, Jinan Lou, Massoud Pedram** -
Univ. of Southern California, Los Angeles, CA



SESSION 8

Room: 305

ENVIRONMENT FOR COLLABORATIVE DESIGN

Chair: *Takahide Inoue* - Sony Corp., Milpitas, CA

Organizers: *Richard Smith, Takahide Inoue*

The design of large systems-on-a-chip introduces some new problems with respect to the management of very diversified design teams including system designers, IP providers and semiconductor chip designer. These designers want to use the best in their class tools but also need to collaborate to make the overall design real. This session introduces some new ideas for very large scale collaborative design environments, H/S codesign and tool encapsulation.

8.1 Framework Encapsulations: A New Approach to CAD Tool Interoperability

Peter Sutton - Queensland Univ. of Tech., Brisbane, Australia

Stephen W. Director - Univ. of Michigan, Ann Arbor, MI

8.2 A Geographically Distributed Framework for Embedded System Design and Validation

Ken Hines, Gaetano Borriello - Univ. of Washington, Seattle, WA

8.3 Weld - An Environment for Web-Based Electronic Design

Francis L. Chan, Mark D. Spiller, A. Richard Newton - Univ. of California, Berkeley, CA

SESSION 9

Room: 304

NEW METHODS IN FUNCTIONAL VERIFICATION

Chair: *Rajesh K. Gupta* - Univ. of California, Irvine, CA

Organizers: *Vivek Tiwari, Kenji Yoshida*

Design verification is one of the most complex and time consuming components of the design process. Functional verification continues to be the most popular method for verifying designs early and often. The papers in this session present methods to improve the speed and effectiveness of functional verification.

§ 9.1 OCCOM: Efficient Computation of Observability-Based Code Coverage Metrics for Functional Verification

Farzan Fallah, Srinivas Devadas - Massachusetts Inst. of Tech., Cambridge, MA

Kurt Keutzer - Univ. of California, Berkeley, CA

9.2 User Defined Coverage - A Tool Supported Methodology for Design Verification

Raanan Grinwald, Eran Harel, Michael Orgad, Shmuel Ur, Avi Ziv - IBM Corp., Haifa, Israel

9.3S Enhanced Visibility and Performance in Functional Verification by Reconstruction

Joshua Marantz - IKOS Systems, Inc., Waltham, MA

9.4S Virtual Chip: Making Functional Models Work on Real Target Systems

Namseung Kim, Hoon Choi, Seungjong Lee, Seungwang Lee, In-Cheol Park, Chong-Min Kyung - KAIST, Taejon, Korea

SESSION 10

Room: 103

PANEL: HARDWARE/SOFTWARE CO-DESIGN - THE NEXT EMBEDDED SYSTEM DESIGN CHALLENGE

Chair: *Pete Heller* - Collett International, Inc., Santa Clara, CA

Organizers: *Diane Orr, Kristin Hehir* - Tsantes & Associates, Campbell, CA

Issues, challenges, tradeoffs and solutions being employed in the design of systems with increasing amounts of functionality implemented in software will be explored in this panel. Perspectives from system designers and tool vendors in hardware and software development domains will be shared. This panel's goal is to identify challenges embedded designers face and determine if design tools offered provide true hardware/software co-design solutions.

Without an interface to synthesis, can hardware/software co-design provide meaningful value? Can automatic hardware and software partitioning tools replace humans? Who is responsible for hardware/software co-design? System architects? Hardware designers? Software designers? Can tools optimize system functionality and performance tradeoffs between hardware and software implementation? Are commercial real time operating systems impacting hardware and software tradeoff decisions?

PANEL MEMBERS:

Guido Arnout - CoWare, Inc., Santa Clara, CA

John Fogelin - Wind River Systems, Alameda, CA

Vess L. Johnson - Omniview Design, Inc., Pittsburgh, PA

Mark Medovich - Sun Microsystems, Palo Alto, CA

Fred Rose - Honeywell, Inc., Minneapolis, MN

James A. Rowson - Alta Group of Cadence Design Systems, Inc.,



Wednesday, June 17

technical program

Sunnyvale, CA

SESSION 11

Room: 102

SYSTEM-LEVEL POWER OPTIMIZATION

Chair: Vivek Tiwari - Intel Corp., Santa Clara, CA
Organizers: Rajesh K. Gupta, Sunil D. Sherlekar

Power optimization at the system level must address a diverse array of issues ranging from choice of system hardware and software components, memory system design and appropriate policies for use of system resources. Papers in this session report on the progress in methodologies, frameworks and policy optimization for power reduction at the system level.

11.1 Power Optimization of Variable Voltage Core-Based Systems

*Inki Hong, Darko Kirovski, **Gang Qu**, Miodrag M. Potkonjak, Mani Srivastava* - Univ. of California, Los Angeles, CA

11.2 Policy Optimization for Dynamic Power Management

*Giuseppe Paleologo, **Luca Benini*** - Stanford Univ., Stanford, CA
Alessandro Bogliolo - Univ. of Bologna, Bologna, Italy
Giovanni De Micheli - Stanford Univ., Stanford, CA

11.3 A Framework for Estimating and Minimizing Energy Dissipation of Embedded HW/SW Systems

Yanbing Li - Princeton Univ., Princeton, NJ

Joerg Henkel - NEC USA, C&C Research Labs., Princeton, NJ

SESSION 12

Room: 301

BOOLEAN METHODS

Chair: Fabio Somenzi - Univ. of Colorado, Boulder, CO

Organizers: Sharad Malik, Randal E. Bryant

This session examines new analysis techniques for Boolean functions. The first paper presents an innovative instance-specific hardware acceleration for SAT formulas using configurable logic. The second paper presents a technique for exact minimization of BDD representations of functions. Finally, the last paper presents a canonical NPN representation of functions for the use in technology mapping.

12.1 Using Reconfigurable Computing Techniques to Accelerate Problems in the CAD Domain: A Case Study with Boolean Satisfiability

Peixin Zhong - Princeton Univ., Princeton, NJ
Pranav Ashar - NEC USA, C&C Research Labs., Princeton, NJ
Sharad Malik, Margaret Martonosi - Princeton Univ., Princeton, NJ

12.2 Fast Exact Minimization of BDDs

Rolf Drechsler, Nicole Drechsler, Wolfgang Günther - Univ. of Freiburg, Freiburg, Germany

12.3 Boolean Matching for Large Libraries

8:30
to
10:00

§ - denotes best paper



Uwe Hinsberger, **Reiner Kolla** - Univ. Wuerzburg, Wuerzburg, Germany

SESSION 13

Room: 305

EXTRACTION AND MODELING FOR INTERCONNECT

Chair: *Hidetoshi Onodera* - Kyoto Univ., Kyoto, Japan

Organizers: *Hidetoshi Onodera, Alan Mantooth*

Fast and accurate analysis of interconnect is crucial for the performance estimation of deep sub-micron circuits. This session discusses methods for interconnect parasitic extraction using integral equation approaches. The first paper presents 3-D capacitance extraction based on a hierarchical algorithm for the N-body problem. The second paper proposes a BEM formulation for generating macromodels used in 2-D hierarchical capacitance extraction. The last paper describes a computationally efficient method for parasitic extraction using a multi layered 3-D Green's function.

§ 13.1 A Fast Hierarchical Algorithm for 3-D Capacitance Extraction

Weiping Shi, *Jianguo Liu, Naveen Kakani* - Univ. of North Texas, Denton, TX
Tiejun Yu - Univ. of North Carolina, Charlotte, NC

13.2 Boundary Element Method Macromodels for 2-D Hierarchical Capacitance Extraction

E. Aykut Dengi - Motorola, Inc., Austin, TX
Ronald A. Rohrer - Intersouth Partners, Research Triangle Park, NC

13.3 Efficient Three-Dimensional Extraction Based on Static and Full-Wave Layered Green's Functions

Jinsong Zhao - Univ. of California, Santa Cruz, CA
Sharad Kapur, David E. Long - Bell Labs., Lucent Tech., Murray Hill, NJ

Wayne W.M. Dai - Univ. of California, Santa Cruz, CA

SESSION 14

Room: 304

PROCESSOR DESIGN AND SIMULATION

Chair: *Randolph E. Harr* - Synopsys, Inc., Mountain View, CA

Organizers: *Anantha Chandrakasan, Randolph E. Harr*

Embedded and single-chip processors are the core element for all new computing platforms. Unique design problems inherent to these processors are finally emerging. This session covers some recent tool and methodology developments applied to the design of DSPs and microprocessors.

14.1 Robust Elmore Delay Models Suitable for Full Chip Timing Verification of a 600 MHz CMOS Microprocessor

Nevine Nassif - Digital Equipment Corp., Hudson, MA
Madhav P. Desai - Indian Inst. of Tech, Powai, Mumbai, India
Dale H. Hall - Digital Equipment Corp., Hudson, MA

14.2 A Top-Down Design Environment for Developing Pipelined Datapaths

Robert M. McGraw - RAM Labs., Encinitas, CA

Robert H. Klenke, James H. Aylor - Univ. of Virginia, Charlottesville, VA

14.3S Validation of an Architectural Level Power Analysis Technique

Rita Yu Chen, Robert M. Owens, Mary Jane Irwin - Penn State Univ., University Park, PA
Raminder S. Bajwa - Hitachi America Ltd., San Jose, CA

14.4S Design Methodology of a 200MHz Superscalar Microprocessor: SH-4

Toshihiro Hattori, Yusuke Nitta,

Mitsuho Seki, *Susumu Narita, Kunio Uchiyama, Tsuyoshi Takahashi, Ryuichi Satomura* - Hitachi Ltd., Tokyo, Japan

SESSION 15

Room: 103

PANEL: HOW MUCH ANALOG DOES A DESIGNER NEED TO KNOW FOR SUCCESSFUL MIXED-SIGNAL DESIGN?

Chair: *Stephan Ohr* - EE Times, Westfield, NJ

Organizers: *Georgia Marszalek* - Marketing Consultant, Foster City, CA
Nanette Collins - Consultant, Boston, MA

With today's mixed-signal designs, there has to be a team of analog and digital designers working on distinct parts of the projects – analog designers need to train themselves as digital designers, or digital designers need to train themselves as analog designers. For mixed-signal design, do analog designers know enough to control voltages and current in digital CMOS or is a different orientation required? Do digital designers know enough about what an analog circuit is supposed to do to replicate its functions in digital CMOS? Are either analog or digital tool sets adequate for mixed-signal design? Is something different required? Can analog designers master high-level design languages? And will this help or hinder the design process?

PANEL MEMBERS:

Bob Dobkin - Linear Technology, Milpitas, CA
Felicia James - Texas Instruments, Dallas, TX
Ken Kundert - Cadence Design Systems, Inc., San Jose, CA
Lavi Lev - Silicon Graphics, Inc., Mountain View, CA
Maqsoodul Mannan - DSM

10:30 to 12:00

§ - denotes best paper

Technologies, San Jose, CA
Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA

SESSION 16 Room: 102

PERFORMANCE MODELING AND CHARACTERIZATION FOR EMBEDDED SYSTEMS

Chair: Sunil D. Sherlekar - Silicon Automation Systems, Bangalore, India

Organizers: Sunil D. Sherlekar, Rajesh K. Gupta

Design of embedded systems, particularly in time-constrained signal processing applications, requires accurate performance characterization. The first two papers present probabilistic characterization of performance and its use in signal processing applications. The last paper addresses the problem of deterministic detailed performance constraints from interface specifications using a deterministic method.

16.1 Hierarchical Algorithms for Assessing Probabilistic Constraints on System Performance

Gustavo De Veciana, **Margarida Jacome**, Jian-Huei Guo - Univ. of Texas, Austin, TX

16.2 A Tool for Performance Estimation of Networked Embedded Systems

Asawaree Kalavade, Pratyush Moghe - Lucent Tech., Bell Labs., Holmdel, NJ

16.3 Rate Derivation and its Applications to Reactive, Real-Time Embedded Systems

Ali Dasdan - Univ. of Illinois-Champaign,

Urbana, IL
Dinesh Ramanathan - Synopsys, Inc., Mountain View, CA
Rajesh K. Gupta - Univ. of California, Irvine, CA

SESSION 17 Room: 301

ADVANCES IN PLACEMENT AND PARTITIONING

Chair: Antun Domic - Synopsys, Inc., Mountain View, CA

Organizers: Patrick Groeneveld, Andrew B. Kahng

This session opens with two powerful advances in the quadratic placement approach. Next, the novel application of placement with incomplete netlist information is introduced. The last two papers address new multi-way partitioning and clustering formulations.

§ 17.1 Generic Global Placement and Floorplanning

Hans Eisenmann, Frank M. Johannes - Technical Univ. of Munich, Munich, Germany

17.2S Congestion Driven Quadratic Placement

Phiroze N. Parakh, Richard B. Brown, Karem A. Sakallah - Univ. of Michigan, Ann Arbor, MI

17.3S Potential_NRG: Placement with Incomplete Data

Maogang Wang, Prithviraj Banerjee, Majid Sarrafzadeh - Northwestern Univ., Evanston, IL

17.4S Performance-Driven Multi-FPGA Partitioning Using Functional Clustering and Replication

Wen-Jong Fang, **Allen C.-H. Wu** - Tsing Hua Univ., Hsinchu, Taiwan ROC



17.5S Multi-Pad Power/Ground Network Design for Uniform Distribution of Ground Bounce

Jaewon Oh, Massoud Pedram - Univ. of Southern California, Los Angeles, CA

SESSION 18

Room: **305**

PARASITIC DEVICE EXTRACTION AND INTERCONNECT MODELING

Chair: David D. Ling - IBM Corp., Yorktown Heights, NY

Organizers: Alan Mantooh, Hidetoshi Onodera

This session includes papers focused on layout extraction. The first paper deals with the extraction and verification of CMOS I/O Circuits, which involves the extraction of SCR's, parasitic bipolar transistors, etc. The next two papers deal with interconnect extraction and modeling. One involves efficient reduced order models for 3-D interconnects. The other involves extraction of frequency dependent behavior for timing analysis.

18.1 Layout Extraction and Verification Methodology for CMOS I/O Circuits

Tong Li, Sung-Mo Kang - Univ. of Illinois, Urbana, IL

18.2 A Mixed Nodal-Mesh Formulation for Efficient Extraction and Passive Reduced-Order Modeling of 3D Interconnects

Nuno Marques - INESC/Cadence European Labs., Lisboa, Portugal
Mattan Kamon, Jacob K. White - Massachusetts Inst. of Tech., Cambridge, MA

L. Miguel Silveira - INESC/Cadence European Labs., Lisboa, Portugal

18.3 Layout Based Frequency Dependent Inductance and Resistance Extraction for On-Chip Interconnect Timing Analysis

Byron Krauter, Sharad Mehrotra - IBM Corp., Austin, TX

SESSION 19

Room: **304**

DESIGN OPTIMIZATION FOR DSP

Chair: James A. Rowson - Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA

Organizers: Anders Forsen, Ivo Bolsens

Computationally intensive DSP problems can be optimized early in the design cycle. These papers show their approaches: interactive optimization at the behavioral level, a methodology based on C++, and an architectural approach for image processing.

19.1 A Methodology for Guided Behavioral-Level Optimization

Lisa Marie Guerra - Rockwell Semiconductor Systems, Newport Beach, CA

Miodrag M. Potkonjak - Univ. of California, Los Angeles, CA

Jan M. Rabaey - Univ. of California, Berkeley, CA

19.2 A Programming Environment for the Design of Complex High Speed ASICs

Patrick R. Schaumont, Serge Vernalde, Luc Rijnders, Marc Engels, Ivo Bolsens - IMEC, Leuven, Belgium

19.3 Media Architecture: General Purpose vs. Multiple Application Specific Programmable Processor

Chunho Lee, **Johnson S. Kin**, Miodrag M. Potkonjak, William H. Mangione-Smith - Univ. of California, Los Angeles, CA

SESSION 20

Room: **103**

PANEL: USER EXPERIENCE WITH HIGH LEVEL FORMAL VERIFICATION

Chair: Gerry Musgrave - Brunel Univ., Uxbridge, UK

Organizers: Gerry Musgrave - Brunel Univ., Uxbridge, UK
Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

Formal verification methods are beginning to be used by leading edge industries. How effective are they, how easy it is to embed them in the design flow and what are the future requirements are questions the industry wishes to have answered. The panel will attempt to answer these and other aspects of model checking or parameter validation techniques by sharing their experience in using a variety of tools. The emphasis will be on what has been achieved and how design teams cope with changes in design flow. They will also describe how they have been able to transform from using the tools as a post design checker to be a proactive design aid in achieving quality designs in a shorter time.

PANEL MEMBERS:

Pierre Aulagnier - Cisco Systems, San Jose, CA

Fumiyasu Hirose - Fujitsu Labs., Ltd., Kawasaki, Japan

Michael Payer - Siemens AG, Munich, Germany

Alan Silbert - Nortel, Ottawa, ON, Canada

John Van Tassel - Texas Instruments, Inc., Dallas, TX



2:00
to
4:00

SESSION 21

Room: 102

BRIDGING THE GAP BETWEEN SIMULATION AND FORMAL VERIFICATION

Chair: *Andreas Kuehlmann* - IBM Corp.,
Yorktown Heights, NY

Organizers: *Randal E. Bryant, Sharad Malik*

Neither of the two extremes of design validation: endless simulation runs over ad hoc tests sets or rigorous mathematical proofs of correctness, represent cost effective methods to ensure quality designs. Instead, it is better to find intermediate approaches combining good engineering practice with the mathematical reasoning capabilities of formal verification. The result can be to either run simulations that will achieve high coverage or to use formal verification tools to analyze critical aspects of the behavior over abstracted system models. This session, consisting of two embedded tutorials, provides an overview of the state of the art and the future opportunities for both of these intermediate approaches.

21.1 Embedded Tutorial: What's Between Simulation and Formal Verification?

David L. Dill - Stanford Univ., Stanford, CA

21.2 Embedded Tutorial: Targeted Formal Verification

Ken McMillian - Cadence Design Systems, Inc.,
Berkeley, CA

SESSION 22

Room: 301

LOGIC OPTIMIZATION

Chair: *Albert Wang* - Synopsys, Inc., Mountain
View, CA

Organizers: *Jason Cong, TingTing Hwang*

This session presents recent advances on various aspects of logic optimization. The first paper presents a novel method for optimal mapping combined with forward retiming to guarantee efficient initial state computation. The second paper presents on-the-fly technology mapping during logic optimization. The third paper presents new techniques for efficient Boolean division. The fourth paper extends efficient delay-optimal mapping techniques for FPGAs to library-based designs. The last paper presents an efficient solution for fanout optimization.

22.1 Optimal FPGA Mapping and Retiming with Efficient Initial State Computation

Jason Cong, Chang Wu - Univ. of California,
Los Angeles, CA

22.2 M32: A Constructive Multilevel Logic Synthesis System

Karem Sakallah, Victor N. Kravets - Univ. of
Michigan, Ann Arbor, MI

22.3 Efficient Boolean Division and Substitution

Shih-Chieh Chang - National Chung-Cheng
Univ., Chiayi, Taiwan ROC

David I. Cheng - Ultima Interconnect Tech.,
Sunnyvale, CA

22.4S Delay-Optimal Technology Mapping by DAG Covering

Yuji Kukimoto, Robert K. Brayton - Univ. of
California, Berkeley, CA



Prashant Sawkar - Intel Corp., Hillsboro, OR

22.5S A Fast Fanout Optimization Algorithm for Near-Continuous Buffer Libraries

David S. Kung - IBM Corp., Yorktown Heights, NY

SESSION 23

Room: 305

ROUTING FOR PERFORMANCE AND CROSSTALK

Chair: Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

Organizers: Patrick Groenveld, Andrew B. Kahng

Routing today is more than making all connections DRC correct in minimum area. In addition a sub-micron router must maximize performance and minimize undesired effects such as crosstalk. This session is dedicated to new methods for routing that optimize for these new concerns.

23.1 Performance Driven Multi-Layer General Area Routing for PCB/MCM Designs

Jason Cong, Patrick H. Madden - Univ. of California, Los Angeles, CA

23.2 Buffer Insertion for Noise and Delay Optimization

Charles J. Alpert, Anirudh Devgan, Stephen T. Quay - IBM Corp., Austin, TX

23.3 Table-Lookup Methods for Improved Performance-Driven Routing

John Lillis - Univ. of Illinois, Chicago, IL
Premal Buch - Magma Design Automation, Inc., Mountain View, CA

23.4S Global Routing with Crosstalk Constraints

Hai Zhou, D.F. Wong - Univ. of Texas, Austin, TX

23.5S Timing and Crosstalk Driven Area

Routing

Hsiao-Ping Tseng - Univ. of Washington, Seattle, WA

Louis Scheffer - Cadence Design Systems, Inc., San Jose, CA

Carl Sechen - Univ. of Washington, Seattle, WA

SESSION 24

Room: 304

PRACTICAL OPTIMIZATION METHODOLOGIES FOR HIGH PERFORMANCE DESIGN

Chair: Vivek Tiwari - Intel Corp., Santa Clara, CA

Organizers: Vivek Tiwari, Kenji Yoshida

The push for high performance design continues to stress the capabilities of conventional tools. This motivates the development of innovative design methodologies. The first paper describes a unified methodology for process and circuit optimization. The other papers present practical solutions for the problems of timing improvement of std cell circuits, repeater insertion and datapath synthesis.

24.1 Process/Multi-Circuit Optimization

Arun N. Lokanathan, Jay B. Brockman - Univ. of Notre Dame, Notre Dame, IN

24.2S Migration: A New Technique to Improve Synthesized Designs Through Incremental Customization

Rajendran V. Panda, Abhijit Dharchoudhury - Motorola, Inc., Austin, TX
Tim Edwards, Joe Norton, David T. Blaauw - Motorola, Inc., Austin, TX

24.3S A Practical Repeater Insertion Method Using Elmore Delay in High Speed VLSI Circuits

Julian Culetu, Chaim Amir, John MacDonald - Sun Microsystems, Inc., Palo Alto, CA

24.4 Practical Experiences with Standard-Cell Based Datapath Design

Tools — Do We Really Need Regular Layouts?

Paolo lenne, Alexander Griessing - Siemens AG, Munich, Germany

24.5 A Statistical Performance Simulation Methodology for VLSI Circuits

Michael Orshansky, James C. Chen, Chenming Hu - Univ. of California, Berkeley, CA

SESSION 25

Room: 103

RF IC DESIGN METHODOLOGY

Chair: Mojoy C. Chian - Harris Semiconductor, Melbourne, FL

Organizers: Bryan D. Ackland, Mojoy C. Chian

RF design has long been considered a black art. Historically design tools have been unable to provide an integrated environment for RF IC design. This session describes specific constraints and challenges faced by RF IC designers and CAD tool developers, including the strong coupling between signal integrity and design.

25.1 Embedded Tutorial: RF IC Design Challenges

Behzad Razavi - Univ. of California, Los Angeles, CA

25.2 Tools and Methodology for RF IC Design

Alfred E. Dunlop, Alper Demir, Peter Feldmann, Sharad Kapur, David E. Long, Robert C. Melville, Jaijeet S. Roychowdhury - Bell Labs., Lucent Tech., Murray Hill, NJ

25.3 Electromagnetic Modeling and Signal Integrity Simulation of Power/Ground Networks in High Speed Digital Packages & Printed Circuit Boards

Frank Y. Yuan - Viewlogic Systems Group, Inc., Camarillo, CA



4:30
to
6:00

SESSION 26

Room: 102

THEORY AND PRACTICE IN HIGH LEVEL SYNTHESIS

Chair: *Steve Tjiang* - Synopsys, Inc., Mountain View, CA

Organizers: *David Ku, Timothy Kam*

This session concentrates on advances in fundamental algorithms and applications for high level synthesis. The first paper presents improvements in graph coloring using a combination of new techniques. The second paper presents a technique of transforming arithmetic circuits into ones using carry-save-adders. The third paper describes a behavioral synthesis system that optimizes for power and area.

26.1 Efficient Coloring of a Large Spectrum of Graphs

Darko Kirovski, Miodrag M. Potkonjak - Univ. of California, Los Angeles, CA

26.2 Arithmetic Optimization Using Carry-Save-Adders

Taewhan Kim - Synopsys, Inc., Mountain View, CA

William Jao - Aimfast Corp., Sunnyvale, CA

Steve Tjiang - Synopsys, Inc., Mountain View, CA

26.3 Synthesis of Power-Optimized and Area-Optimized Circuits from Hierarchical Behavioral Descriptions

Ganesh Lakshminarayana, Niraj K. Jha - Princeton Univ., Princeton, NJ

SESSION 27

Room: 301

BDD APPROXIMATION TECHNIQUES

Chair: *Andreas Kuehlmann* - IBM Corp., Yorktown Heights, NY

Organizers: *Andreas Kuehlmann, Kunle Olukotun*

This session presents three papers that use approximation and decomposition of BDD's to enhance the current state of the art in reachability analysis.

27.1 Approximation and Decomposition of Binary Decision Diagrams

Kavita Ravi - Univ. of Colorado, Boulder, CO

Kenneth L. McMillan - Cadence Design Systems, Inc., Berkeley, CA

Thomas R. Shiple - Synopsys, Inc., Mountain View, CA

Fabio Somenzi - Univ. of Colorado, Boulder, CO



27.2 Approximate Reachability with BDDs Using Overlapping Projections

Shankar G. Govindaraju, David L. Dill - Stanford Univ., Stanford, CA
Alan J. Hu - Univ. of British Columbia, Vancouver, BC, Canada
Mark A. Horowitz - Stanford Univ., Stanford, CA

27.3 Incremental CTL Model Checking Using BDD Subsetting

Abelardo Pardo - Mentor Graphics Corp., Billerica, MA
Gary D. Hachtel - Univ. of Colorado, Boulder, CO

SESSION 28

Room: **305**

INTERCONNECT MODELING AND TIMING SIMULATION

Chair: Andrew T. Yang - Univ. of Washington, Seattle, WA

Organizers: Andrew T. Yang, Hidetoshi Onodera

Non-linear electrical-level circuit and timing simulation play an important role in the design and analysis of large scale ICs. The first three papers in this session address a variety of interconnect modeling techniques which can be used in circuit simulation and timing analysis. The last paper presents a method for computing adjoint transient sensitivity in an event-driven PWL simulator.

28.1 Primo: Probability Interpretation of Moments for Delay Calculation

Rony Kay, **Lawrence T. Pileggi** - Carnegie Mellon Univ., Pittsburgh, PA

28.2S FTD: An Exact Frequency to Time Domain Conversion for Reduced Order RLC Interconnect Models

Ying Liu, Lawrence T. Pileggi, Andrzej J. Strjwas - Carnegie Mellon Univ.,

Pittsburgh, PA

28.3S Extending Moment Computation to 2-Port Circuit Representations

Fang-Jou Liu, Chung-Kuan Cheng - Univ. of California, San Diego, La Jolla, CA

28.4 Adjoint Transient Sensitivity Computation in Piecewise Linear Simulation

Tuyen V. Nguyen, Anirudh Devgan - IBM Corp., Austin, TX
Ognen J. Nastov - Massachusetts Inst. of Tech., Cambridge, MA

SESSION 29

Room: **304**

LOW POWER DESIGN USING MULTIPLE THRESHOLDS AND SUPPLIES

Chair: Bryan D. Ackland - Bell Labs., Lucent Tech., Holmdel, NJ

Organizers: Anantha Chandrakasan, Bryan D. Ackland

Techniques for optimally assigning supply voltage and selecting threshold voltages so as to provide desired tradeoff between performance, active power and standby power dissipation are presented.

29.1 Design Methodology of Ultra Low-Power MPEG4 Codec Core Exploiting Voltage Scaling Techniques

Kimiyoshi Usami, Mutsunori Igarashi, Takashi Ishikawa, Masahiro Kanazawa, Masafumi Takahashi, Mototsugu Hamada, Hideho Arakida, Toshihiro Terazawa, Tadahiro Kuroda - Toshiba Corp., Kawasaki, Japan

29.2 Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits

Liqiong Wei, Zhanping Chen, **Kaushik Roy**, Vivek De - Purdue Univ., West Lafayette, IN

29.3 MTCMOS Hierarchical Sizing Based on Mutual Exclusive Discharge Patterns

James Kao, Siva Narendra, Anantha Chandrakasan - Massachusetts Inst. of Tech., Cambridge, MA

SESSION 30

Room: **103**

PANEL: TECHNICAL CHALLENGES OF IP AND SYSTEM-ON-CHIP: THE ASIC VENDOR PERSPECTIVE

Chair: Richard Newton - Univ. of California, Berkeley, CA

Organizers: Andrew Graham - Si2, Austin, TX
Andrew B. Kahng - Univ. of California, Los Angeles, CA

The demand for system-on-chip solutions is creating vast changes in reuse methodology and EDA technology. Traditional roles of foundries, ASIC suppliers, and EDA vendors are blurring. For the end customer, the situation presents correspondingly greater risks and opportunities. This panel brings together today's leading providers of embedded silicon IP solutions. The panelists will discuss practical expectations for system-on-chip design, and the key pieces of industry infrastructure that must be addressed to realize the full potential of system-on-chip. These include: customer expectations, EDA technology implications; standards; legal barriers and associated risks facing ASIC suppliers and EDA vendors; challenges of incorporating 3rd-

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Thursday, June 18

technical
program8:30
to
10:00§ - denotes
best paper

party IP; and practical reuse methodologies.

PANEL MEMBERS:

Bruce Beers - IBM Corp., Essex Junction, VT

Jeffery Hilbert - LSI Logic, Milpitas, CA

Michael Jackson - Motorola, Inc., Austin, TX

Anand Naidu - Sand Microelectronics, Santa Clara, CA

Bob Payne - VLSI Technology,

San Jose, CA

Mark Stibitz - Lucent Technologies, Allentown, PA

Hitoshi Yoshizawa - NEC Corp., Kawasaki, Japan

Luciano Lavagno - Cadence Design Systems, Inc., Berkeley, CA

Ellen M. Sentovich - Cadence Berkeley Labs., Berkeley, CA

31.3 Instruction Selection, Resource Allocation, and Scheduling in the AVIV Retargetable Code Generator

Silvina Hanono, Srinivas Devadas - Massachusetts Inst. of Tech., Cambridge, MA

31.4 Code Compression for Embedded Systems

Haris Lekatsas, Wayne Wolf - Princeton Univ., Princeton, NJ

SESSION 31Room: **102****SOFTWARE SYNTHESIS AND RETARGETABLE COMPILATION**

Chair: *Kurt Keutzer* - Univ. of California, Berkeley, CA

Organizers: *Luciano Lavagno, Sharad Malik*

This session explores aggressive techniques for meeting tight space and time constraints for embedded software. These are applicable at different levels of the design process. At the high level, these include C-code synthesis with quasi-static scheduling, as well as don't care based optimization. At compile time, the next paper explores integrated instruction selection, resource allocation and data routing for parallel architectures. Finally, the last paper examines how compressed code can be used with runtime decompression to achieve code size reduction.

31.1S Software Synthesis of Process-Based Concurrent Programs

Bill Lin - Univ. of California, San Diego, La Jolla, CA

31.2S Don't Care-Based BDD Minimization for Embedded Software

Youpyo Hong, Peter Beerel - Univ. of Southern California, Los Angeles, CA

SESSION 32Room: **301****FORMAL METHODS IN FUNCTIONAL VERIFICATION**

Chair: *Kunle Olukotun* - Stanford Univ., Stanford, CA

Organizers: *Kunle Olukotun, Andreas Kuehlmann*

This session explores techniques for functional-level verification. The first paper adds support for bit-vector arithmetic to a formal verification environment that combines theorem proving and model checking. The second paper presents a new technique for generating functional test vectors. The last two papers demonstrate the industrial use of symbolic trajectory evaluation.

§ 32.1 A Decision Procedure for Bit-Vector Arithmetic

Clark W. Barrett, David L. Dill, Jeremy R. Levitt - Stanford Univ., Stanford, CA

32.2 Functional Vector Generation for HDL Models Using Linear Programming and 3-Satisfiability



Farzan Fallah, Srinivas Devadas - Massachusetts Inst. of Tech., Cambridge, MA
Kurt Keutzer - Univ of California, Berkeley, CA

32.3S Automatic Generation of Assertions for Formal Verification of PowerPC Microprocessor Arrays Using Symbolic Trajectory Evaluation

Li-C. Wang, Magdy S. Abadir, Nari Krishnamurthy - Motorola, Inc., Austin, TX

32.4S Combining Theorem Proving and Trajectory Evaluation in an Industrial Environment

Mark D. Aagaard, Robert B. Jones, Carl-Johan H. Seger - Intel Corp., Hillsboro, OR

SESSION 33

Room: 305

CORE TEST AND BIST

Chair: *Janusz Rajski* - Mentor Graphics Corp., Wilsonville, OR

Organizers: *Yervant Zorian, Janusz Rajski*

This session addresses test issues at higher-levels of design abstraction. The papers introduce new methodologies for testing of core-based systems and optimized BIST schemes inserted at register transfer and behavioral levels.

33.1 A Fast and Low Cost Testing Technique for Core-Based System-on-a-Chip

Indradeep Ghosh - Princeton Univ., Princeton, NJ
Sujit Dey - Univ. of California, San Diego, La Jolla, CA
Niraj K. Jha - Princeton Univ., Princeton, NJ

33.2 Introducing Redundant Computations in a Behavior for Reducing BIST Resources

Ishwardutt Parulkar - Sun Microsystems, Sunnyvale, CA
Sandeep K. Gupta, Melvin A. Breuer - Univ. of Southern California, Los Angeles, CA

33.3 A BIST Scheme for RTL Controller-Data Paths Based on Symbolic Testability Analysis

Indradeep Ghosh, Niraj K. Jha - Princeton Univ., Princeton, NJ
Sudipta Bhawmik - Bell Labs., Lucent Tech., Princeton, NJ

SESSION 34

Room: 304

INTERCONNECT ANALYSIS AND RELIABILITY IN DEEP SUB-MICRON

Chair: *Kenji Yoshida* - Toshiba Corp., Kawasaki, Japan

Organizers: *Kenji Yoshida, David T. Blaauw*

In designing deep sub-micron LSIs, new issues need to be carefully considered for high performance and reliability. In this session, design considerations and analysis of inductance and electromigration of deep sub-micron interconnect will be discussed.

34.1 Figures of Merit to Characterize the Importance of On-Chip Inductance

Yehea I. Ismail, Eby G. Friedman - Univ. of Rochester, Rochester, NY
Jose L. Neves - IBM Corp., East Fishkill, NY

34.2 Layout Techniques for Minimizing On-Chip Interconnect Self Inductance

Yehia Massoud - Massachusetts Inst. of Tech., Cambridge, MA
Steve Majors - Rockwell Semiconductor

Systems, Austin, TX
Tareq Bustami - Motorola Inc., Austin, TX
Jacob K. White - Massachusetts Inst. of Tech., Cambridge, MA

34.3 A Practical Approach to Static Signal Electromigration Analysis

Nagaraj NS - Texas Instruments Inc., Dallas, TX
Frank Cano, Haldun Haznedar, Duane Young - Texas Instruments Inc., Stafford, TX

SESSION 35

Room: 103

PANEL: DESIGN PRODUCTIVITY: HOW TO MEASURE IT, HOW TO IMPROVE IT

Chair: *Carlos Dangelo* - Semiconductor Research Corp., San Jose, CA

Organizers: *Ronald E. Collett* - Collett International, Inc., Santa Clara, CA

Andrew B. Kahng - Univ. of California, Los Angeles, CA

This panel will discuss factors that have the greatest impact on design productivity and time-to-market. Panelists will review the practices and strategies that they use today to improve productivity and time-to-market (impact of EDA tools, library strategy, design team composition and dynamics, etc.), as well as the results of these practices and strategies. The panel will also discuss and present approaches to measuring productivity, from both a quantitative and qualitative perspective. Questions that will be addressed include the following. (1) What kind of measurements, if any, are being used today? (2) What have been the results? (3) Are they useful? (4) Is there a consensus about the kinds of measurements that should be taken? (5) What kind of metrics are needed?

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Thursday, June 18

technical program

10:30
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Thursday
Keynote
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1:00 to 1:45
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Keynote

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best paper

PANEL MEMBERS:

Andy Bechtolsheim - Cisco Systems, San Jose, CA
Ronald E. Collett - Collett International, Santa Clara, CA
Jeff Hilbert - LSI Logic, Milpitas, CA
Chris Malachowsky - NVidia Corp., Sunnyvale, CA
Leif Rosqvist - Cadence Spectrum Design, San Jose, CA
Jim Thomas - Motorola M-Core Technology Ctr., Austin, TX

SESSION 36

Room: 102

HIERARCHICAL FUNCTIONAL TIMING ANALYSIS

Chair: *Tom Szymanski* - Bell Labs., Lucent Tech., New Providence, NJ
Organizers: *Sharad Malik, Farid N. Najm*

This session examines new techniques in timing analysis at various levels of abstraction: accurate modeling for interconnect analysis; hierarchical modeling and analysis at the gate level; register transfer level timing estimation and analysis of system level timing diagrams.

36.1 Hierarchical Functional Timing Analysis
Yuji Kukimoto, Robert K. Brayton - Univ. of California, Berkeley, CA

36.2 Making Complex Timing Relationships Readable: Presburger Formula Simplification Using Don't Cares

Tod Amon - Southwest Texas State Univ., San Marcos, TX
Gaetano Borriello - Univ. of Washington, Seattle, WA
Jiwen Liu - Southwest Texas State Univ., San Marcos, TX

36.3S Delay Estimation of VLSI Circuits from a High-Level View

Mahadevamurty Nemani, Farid N. Najm - Univ. of Illinois, Urbana, IL

36.4S TETA: Transistor-Level Engine for Timing Analysis

Florentin Dartu, Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

SESSION 37

Room: 301

NEW TECHNIQUES IN STATE SPACE EXPLORATIONS

Chair: *Carl-Johan H. Seger* - Intel Corp., Hillsboro, OR
Organizers: *Andreas Kuehlmann, Kunle Olukotun*

This session presents four verification approaches based on state space exploration. The first paper describes a search scheme to uncover bad reachable states. The next two papers present verification methods which are based on classifying the state space of systems. The last paper describes a method for test case generation which cause heavy controller interactions.

37.1 Validation with Guided Search of the State Space

C. Han Yang, David L. Dill - Stanford Univ., Stanford, CA

37.2 Efficient State Classification of Finite



State Markov Chains

Aiguo Xie, Peter A. Beerel - Univ. of Southern California, Los Angeles, CA

37.3S An Implicit Algorithm for Finding Steady States and its Application to FSM Verification

Gagan Hasteer - Ambit Design Systems, San Jose, CA
Anmol Mathur - Silicon Graphics Corp., Mountain View, CA

Prithviraj Banerjee - Northwestern Univ., Evanston, IL

37.4S Hybrid Verification Using Saturated Simulation

Adnan Aziz - Univ. of Texas, Austin, TX
Thomas R. Shiple, James H. Kukula - Synopsys, Inc., Mountain View, CA

SESSION 38

Room: 305

ADVANCED ATPG TECHNIQUES

Chair: *Yervant Zorian* - LogicVision, Inc., San Jose, CA

Organizers: *Yervant Zorian, Janusz Rajski*

Advanced techniques developed for automatic test pattern generation frequently find applications in design verification. Papers presented in this session introduce new efficient techniques to generate input/output sequences for functional testing, new high-performance method for sequential learning of implications and a fault simulation-based method for diagnosing general design errors in sequential circuits.

38.1 Fast State Verification

Bapiraju Vinnakota, Dechang Sun, Wanli Jiang - Univ. of Minnesota, Minneapolis, MN

38.2 A Fast Sequential Learning Technique for Real Circuits with Application to Enhancing ATPG Performance

Aiman H. El-Maleh, Mark A. Kassab, Janusz Rajski - Mentor Graphics Corp., Wilsonville, OR

38.3 General Design Error Diagnosis for Sequential Circuits

Shi-Yu Huang - National Semiconductor Corp., Santa Clara, CA
Kwang-Ting Cheng - Univ. of California, Santa Barbara, CA
Kuang-Chien Chen - Verplex Systems, Inc., Fremont, CA
Juin-Yeu Lu - National Semiconductor Corp., Santa Clara, CA

SESSION 39

Room: 304

PRACTICAL EXPERIENCE OF FUNCTIONAL VERIFICATION FOR COMPLEX ICs

Chair: *Rajesh Raina* - Motorola, Inc., Austin, TX

Organizers: *David T. Blaauw, Kenji Yoshida*

Functional verification of large ICs is consuming an increasingly large portion of the design resource and design time. This session examines experiences and results with functional verification methods of two high-performance microprocessor designs and a large ASIC design.

§ 39.1 Functional Verification of a Multiple-Issue, Out-of-Order, Superscaler Alpha Processor—The DEC Alpha 21264 CPU Chip

Michael Quinn, Scott Taylor, Darren Brown, Nathan Dohm, Scot Hildebrandt, James Huggins, Carl Ramey - Digital

Equipment Corp., Hudson, MA

39.2 Design Reliability - Estimation Through Statistical Analysis of Bug Discovery Data

Yossi Malka, Avi Ziv - IBM Corp., Haifa, Israel

39.3 Functional Verification of Large ASICs

Adrian Evans, Allan Silburt, Gary Vrckovnik, Thane Brown, Mario Dufresne, Geoffrey Hall, Tung Ho, Ying Liu - Nortel, Ottawa, ON, Canada

SESSION 40

Room: 103

PANEL: THE EDA STARTUP EXPERIENCE: THE FIRST PRODUCT

Chair: *Erach Desai* - SoundView Financial Group, Inc., Austin, TX

Organizer: *Mike Murray* - Acuson Corp., Mountain View, CA

How does a novel EDA idea get transformed into a commercially successful product? Six veteran EDA entrepreneurs will discuss their experiences in bringing their companies' first products to market. Where did their ideas come from? How did they know their ideas would meet real customer needs? And how many customers would there be? How are evolutionary and revolutionary products developed and marketed differently? When did the entrepreneurs stop developing and start shipping? Who were their competitors and their partners? Did they adopt industry standards or create new ones? How did they use advertising, DAC, and the WWW to promote the product? What are the relative merits of direct, VAR, and OEM selling?

PANEL MEMBERS:

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Thursday, June 18

technical
program2:00
to
4:00

Rick Carlson - Synplicity, Inc., Sunnyvale, CA
Lorne Cooper - Sente, Inc., Acton, MA
Dean Drako - Design Acceleration, Inc., San Jose, CA
Rajeev Madhavan - Magma Design Automation, Inc., Palo Alto, CA
John Sanguinetti - Chronologic, Los Altos, CA
Curt Widdoes - 0-In Design Automation, Inc., San Jose, CA

SESSION 41Room: **102****FAST FUNCTIONAL SIMULATION**

Chair: *Patrick C. McGeer* - Cadence Berkeley Labs., Berkeley, CA

Organizers: *Rajesh K. Gupta, David Ku*

Papers in this session examine recent advances in

fast functional simulation. We begin with an embedded tutorial followed by two short papers demonstrating efficient simulation methods using hybrid modeling and reconfigurable hardware.

41.1 Embedded Tutorial: System Simulation: Methodologies and Examples

Kunle Olukotun, *Mark Heinrich, David Ofelt* - Stanford Univ., Stanford, CA

41.2S Hybrid Techniques for Fast Functional Simulation

Yufeng Luo - Synopsys, Inc., Mountain View, CA
Tjahjadi Wongsonegoro, Adnan Aziz - Univ. of Texas, Austin, TX

41.3S A Reconfigurable Logic Machine for Fast Event-Driven Simulation

Jerry Bauer, Michael Bershteyn, Ian Kaplan, Paul Vyedin - Quickturn Design Systems, Inc., San Jose, CA

SESSION 42Room: **301****POWER ESTIMATION AND MODELING**

Chair: *Farid N. Najm* - Univ. of Illinois, Urbana, IL
Organizers: *Farid N. Najm, Andrew T. Yang*

State of the art integrated circuits are known to dissipate large amounts of power. In order to manage the power dissipation during the design process, CAD approaches are required to estimate and model the power at all levels of abstraction. The papers in this session cover a variety of topics, including parallelized and statistical simulation-based power estimation, high-level power macromodeling, maximum power estimation, and low-power signal encoding.

42.1 Parallel Algorithms for Power Estimation

Victor Kim, *Prithviraj Banerjee* - Northwestern Univ., Evanston, IL

42.2 A Novel Power Macromodeling Technique Based on Power Sensitivity

Zhanping Chen, *Kaushik Roy* - Purdue Univ., West Lafayette, IN



42.3 Maximum Power Estimation Using the Limiting Distributions of Extreme Order Statistics

Qinru Qiu, Qing Wu, Massoud Pedram - Univ. of Southern California, Los Angeles, CA

42.4S An Optimization-Based Error Calculation for Statistical Power Estimation of CMOS Logic Circuits

Byunggyu Kwak - Samsung Data Systems., Seoul, Korea
Eun Sei Park - Hanyang Univ., Kyunggi-do, Korea

42.5S Using Complimentation and Resequencing to Minimize Transitions

Rajeev Murgai, Masahiro Fujita - Fujitsu Labs. of America, Inc., Santa Clara, CA
Arlindo Oliveira - Cadence Eur Labs./INESC/IST, Lisboa, Portugal

SESSION 43

Room: **305**

TECHNOLOGY MAPPING FOR PROGRAMMABLE LOGIC

Chair: *Jonathan Rose* - Univ. of Toronto, Toronto, ON, Canada

Organizers: *Jason Cong, TingTing Hwang*

This session presents new technology mapping algorithms for complex PLDs and FPGAs. The first paper presents synthesis and mapping methods for PLA-style logic blocks. The second and third papers study the technology mapping problems for FPGAs with heterogeneous LUTs. The fourth paper presents a new function decomposition formulation and solution. The fifth and sixth papers present post-layout re-synthesis methods for power reduction in FPGA designs.

43.1 Technology Mapping for Large Complex PLDs

Jason Helge Anderson, Stephen Dean Brown - Univ. of Toronto, Toronto, ON, Canada

43.2S Delay-Optimal Technology Mapping for FPGAs with Heterogeneous LUTs

Jason Cong, Songjie Xu - Univ. of California, Los Angeles, CA

43.3S Exact Tree Based FPGA Technology Mapping for Logic Blocks with Independent LUTs

Madhukar K. Korupolu, K.K. Lee, D.F. Wong - Univ. of Texas, Austin, TX

43.4 Compatible Class Encoding in Hyper-function Decomposition for FPGA Synthesis

Jie-Hong Jiang, Jing-Yang Jou, Juinn-Dar Huang - National Chiao Tung Univ., Hsinchu, Taiwan ROC

43.5S In-Place Power Optimization for LUT-Based FPGAs

Balakrishna Kumthekar - Univ. of Colorado, Boulder, CO

Luca Benini - Univ. of Bologna, Bologna, Italy

Enrico Macii - Politecnico di Torino, Torino, Italy

Fabio Somenzi - Univ. of Colorado, Boulder, CO

43.6S A Re-Engineering Approach to Low Power Design Using SPFD

Janmin Hwang, Fengyi Chiang, TingTing Hwang - Tsing Hua Univ., Hsinchu, Taiwan ROC

SESSION 44

Room: **304**

POWER DISSIPATION AND DISTRIBUTION IN HIGH PERFORMANCE PROCESSORS

Chair: *David T. Blaauw* - Motorola, Inc., Austin, TX

Organizers: *Anatha Chandrakasan, Jan M. Rabaey*

As feature sizes shrink and clock rates grow, power dissipation is rapidly becoming a limiting factor. Sources of power dissipation and power management techniques for high performance processors will be discussed. With high power levels, also comes the challenge of reliably distributing power on the chip.

44.1 Power Considerations in the Design of the Alpha 21264 Microprocessor

Michael K. Gowan, Larry L. Biro, Daniel B. Jackson - Digital Equipment Corp., Hudson, MA

44.2 Reducing Power in High-Performance Microprocessors

Vivek Tiwari, Deo Singh, Suresh Rajgopal, Gaurav Mehta, Junju Sugisawa, Franklin Baez - Intel Corp., Santa Clara, CA

44.3 Design and Analysis of Power Distribution Networks in PowerPC™ Microprocessor

Abhijit Dharchoudhury, Rajendran V. Panda, David T. Blaauw, Ravi Vaidyanathan - Motorola, Inc., Austin, TX
Bogdan Tutuianu, David Bearden - Somerset Design Center, Austin, TX

44.4 Full-Chip Verification Methods for DSM Power Distribution Systems

Gregory Steele - Simplex Solutions, Inc., Sunnyvale, CA

David Overhauser - Simplex Solutions, Inc., San Jose, CA

Steffen Rochel - Simplex Solutions, Inc., Sunnyvale, CA

Syed Zakir Hussain - Simplex Solutions, Inc., San Jose, CA

SESSION 45

Room: **103**

TEST CHALLENGES IN THE SYSTEM CHIP ERA

Chair: *Prab Varma* - Duet Technologies, San Jose, CA

Organizers: *Prab Varma* - Duet Technologies Inc., San Jose, CA
Takahide Inoue - Sony Corp., Milpitas, CA

45.1 Embedded Tutorial: System-Chip Test Strategies

Yervant Zorian - LogicVision, Inc., San Jose, CA

PANEL: System Chip Test Challenges: Are There Solutions Today

The panel will discuss the challenges associated with testing system chips containing pre-designed virtual components and will address the question of whether there are viable solutions today. It will



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Thursday, June 18

technical
program4:30
to
6:00

discuss whether the time to market gains offered by design re-use will be realized without test re-use. It will also debate the impact of the SIA Roadmap on test requirements and the limitations in ATE and the issues in performance testing that will have to be addressed to test tomorrow's system chips.

PANEL MEMBERS:

Sujit Dey - Univ. of California, San Diego, CA
Rudy Garcia - Schlumberger Technologies, San Jose, CA
Erik Jan Marinissen - Philips Research Labs., Eindhoven, The Netherlands
Bruce Mathewson - Advanced RISC Machines Ltd., Cambridge, UK
Rob Roy - Intel Corp., Hillsboro, OR
Prab Varma - Duet Technologies, San Jose, CA
Yervant Zorian - LogicVision, Inc., San Jose, CA

SESSION 46

Room: 102

**CONTROLLER
DECOMPOSITION FOR
POWER AND AREA
MINIMIZATION**

Chair: *Fabio Somenzi* - Univ. of Colorado, Boulder, CO

Organizers: *Timothy Kam, Luciano Lavagno*

Decomposition of finite state controllers is essential to minimize both area and power. The first two papers are devoted to identification and separation of high- and low-activity portions of a finite state machine, respectively at the state graph and at the logic level, in order to significantly increase the opportunities for clock gating. The third paper tackles a classical problem, decomposition for minimum area, by exploiting a hierarchical grammar-based specification

style, and providing partitioned controllers that are easier to understand and debug.

46.1 Finite State Machine Decomposition for Low Power

Jose Monteiro - INESC/IST, Lisboa, Portugal
Arlindo Oliveira - Cadence Eur Labs./INESC/IST, Lisboa, Portugal

46.2 Computational Kernels and Their Application to Sequential Power Optimization

L. Benini, Giovanni De Micheli - Stanford Univ., Stanford, CA
Antonio Liroy, Enrico Macii, G. Odasso, Massimo Poncino - Politecnico di Torino, Torino, Italy

46.3 Partitioning and Optimizing Controllers Synthesized from Hierarchical High-Level Descriptions

Andrew Seawright, Wolfgang Meyer - Synopsys, Inc., Mountain View, CA

SESSION 47

Room: 301

**IP PROTECTION
TECHNOLOGIES**

Chair: *Tom VandenBerge* - Texas Instruments, Dallas, TX

Organizers: *Richard Smith, Takahide Inoue*

The requirement for the exchange of Intellectual Property in the design of systems on a chip is well documented. Protection of IP is needed to support this exchange. This session presents techniques for watermarking IP to prove ownership and encrypting IP to discourage reverse engineering.

47.1 Watermarking Techniques for Intellectual Property Protection

Gregory Wolfe, Miodrag M. Potkonjak, John Lach, William H. Mangione-Smith, Andrew B. Kahng, Stefanus Mantik, Paul Tucker, Huijuan Wang - Univ. of California, Los Angeles, CA
Igor L. Markov - Univ. of California, Beverly Hills, CA

47.2 Robust IP Watermarking Methodologies for Physical Design

Andrew B. Kahng, Stefanus Mantik - Univ. of



California, Los Angeles, CA
Igor L. Markov - Univ. of California, Beverly Hills, CA
Miodrag M. Potkonjak - Univ. of California, Los Angeles, CA
Paul Tucker - Univ. of California, San Diego, CA
Huijuan Wang, Gregory Wolfe - Univ. of California, Los Angeles, CA

47.3 Data Security for Web-Based CAD
Scott Hauck, Stephen Knol - Northwestern Univ., Evanston, IL

SESSION 48

Room: 305

CASE STUDIES OF NEW DESIGN METHODS

Chair: *Anders Forsen* - Ericsson Radio Systems AB, Stockholm, Sweden

Organizers: *Ivo Bolsens, James A. Rowson*

New methods are difficult to evaluate without real data. The papers in this session provide real case studies and benchmarking approaches for four novel design methods.

48.1 Design of a SPDIF Receiver Using Protocol Compiler

Ulrich Holtmann - Synopsys, Inc., Mountain View, CA
Peter Blinzer - Technical Univ. of Braunschweig, Braunschweig, Germany

48.2S Metacore: An Application Specific DSP Development System

Jin-Hyuk Yang, Byung-Woon Kim, Sang-Jun Nam, Jang-Ho Cho, Sung-Won Seo, Chang-Ho Ryu, Young-Su Kwon, Dae-Hyun Lee, Jong-Yeol Lee, Jong-Sun Kim, Hyun-Dong Yoon, Jae-Yeol Kim, Kun-Moo Lee, Chan-Sik Hwang, In-Jung Hwang,

Jun-Sung Kim, Kwang-Il Park, Kyu-Ho Park, Yong-Hoon Lee, Seung-Ho Hwang, In-Cheol Park, Chong-Min Kyung - KAIST, Taejeon, Korea

48.3S A Case Study in Embedded System Design: An Engine Control Unit

Attila Jurecska, Antonino Damiano - Magneti Marelli, Venaria Reale, Italy
Tullio Cuatto, Claudio Passerone, Luciano Lavagno, Claudio Sansoe - Politecnico di Torino, Torino, Italy
Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

48.4S HW/SW Coverification Performance Estimation & Benchmark for a 24 Embedded Risc Core Design

Thomas W. Albrecht, Johann Notbauer, Stefan Rohringer - Siemens AG, Vienna, Austria

48.5S System-Level Exploration with SpecsSyn

Daniel D. Gajski - Univ. of California, Irvine, CA
Frank Vahid - Univ. of California, Riverside, CA
Sanjiv Narayan - Ambit Design Systems, Inc., Santa Clara, CA
Jie Gong - Motorola, Inc., Tempe, AZ

SESSION 49

Room: 103

THIRTY-FIVE YEARS OF DESIGN AUTOMATION, A RETROSPECTIVE AND A LOOK-FOWARD

(no badge is required to attend)

Chair: *Paul Weil* - Intel Corp., Santa Clara, CA

Organizer: *Jan M. Rabaey*

This session will celebrate thirty five years of design automation with three presentations by long time contributors to the field. These presentations will review the past accomplishments and views of the future. There will be a panel session after the talks.

49.1 CAD Through EDA to RIP

Ron Rohrer - Intersouth Partners, Research Triangle Park, NC

49.2 Physical Design Automation: A Look Back and the Challenges Ahead

Bryan Preas - Xerox Parc, Palo Alto, CA

49.3 The New Frontier: From Logic Synthesis to System Design

Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA



Tutorials will be held at the Moscone Center in the Esplanade Ballrooms 301-306.

8:00 AM - Tutorial Registration Opens (Esplanade Lobby)

12:00 Noon - Lunch

8:30 AM - Continental Breakfast

5:00 PM - Tutorials End

9:00 AM - Tutorials Begin

Design Validation Techniques

Room 305

Organizer: *Gitanjali Swamy* - Boston Advanced Development Labs., Mentor Graphics Corp., Boston, MA

Presenters:

Adnan Aziz - Univ. of Texas, Austin, TX

Rajeev Muragi - Fujitsu Labs. of America, Inc., Santa Clara, CA

Amit Narayan - Univ. of California, Berkeley, CA

Gitanjali Swamy - Boston Advanced Development Labs., Mentor Graphics, Boston, MA

Audience: The tutorial will be of interest to the following audiences.

Digital designers, and design project managers: in understanding and choosing validation techniques that are best suited for different design stages. This will assist evaluation of commercial validation offerings, and help devise a comprehensive validation strategy in which bugs are caught early in the design cycle.

CAD vendors: in identifying technologies that are relatively mature in the research community and are ready to be commercialized.

Researchers: in identifying open research problems, where significant advances can be made.

What distinguishes this tutorial from previous ones is that it provides a complete and comprehensive survey of methods for functional validation, rather than focus on a particular technology alone.

Description: The increasing complexity of VLSI systems has made their functional validation extremely difficult. Indeed, verification has become the bottleneck in the IC design process today, with validation teams often being comparable in size to design teams. This tutorial covers state-of-the-art validation techniques. These include the traditional methods of simulation and emulation, as well as the emerging formal verification technologies. We will summarize many of the university CAD tools that incorporate these ideas.

Specifically, the tutorial will cover the following topics: Computational models for designs, State-of-the-art simulation techniques, Emulation technology, Formal equivalence of combinational and sequential gate and RTL level designs, Formal property verification using model checking, language containment, symbolic trajectory evaluation and theorem proving. Techniques for advancing the frontiers of verification ranging from approximation techniques to combining formal verification with simulation for better coverage. Theory will be reinforced by practice through the use of software demonstrations of public domain tools. Emphasis will be placed on techniques which can handle large scale designs.



Tutorial
TwoDesign of Complex Mixed-Signal
Systems on a Chip

Room 302

Organizer: *Ken Kundert* - Cadence Design Systems, Inc., San Jose, CA

Presenters:

Henry Chang - Cadence Design Systems, San Jose, CA

Felicia James - Texas Instruments, Dallas, TX

Dan Jefferies - Cadence Design Systems, Inc., San Jose, CA

Ken Kundert - Cadence Design Systems, Inc., San Jose, CA

Lee Stoian - SiPCore, San Jose, CA

Richard Trihy - Cadence Design Systems, Inc., San Jose, CA

Audience: The primary audience would be circuit designers and CAD engineers involved in complex mixed-signal design.

Description: Shrinking transistor sizes and product lifetimes require engineers to design chips that contain more and more of the system while doing so in less and less time. As more of the system is included on a single chip, it is increasingly likely that that chip will contain both analog and digital sections. These systems are often quite large and complex. For example, a modern read channel IC may have in excess of fifty thousand digital gates and ten thousand analog transistors. In order to manage these more complex designs, many development teams are finding they need to move from traditional "bottom-up" design approaches to more system-oriented "top-down" design style with verification using "mixed-level" simulation. Difficulties in designing and verifying these designs will be discussed and an evolving methodology for reliably designing these large mixed-signal chips with a minimum number of design turns is presented.

In 1998 and 1999 several commercial implementations of the Verilog-AMS and VHDL-AMS standards are expected to become available. Both the Verilog-AMS and VHDL-AMS languages are introduced and contrasted using simple examples. Features and pitfalls are identified. Mixed-level verification using V*-AMS is discussed.

Tutorial
ThreeCAD for System Design: Models, Issues,
and Some Emerging Tools

Room 303

Organizer: *Gaetano Borriello* - Univ. of Washington, Seattle, WA

Presenters:

Gaetano Borriello - Univ. of Washington, Seattle, WA

Jan M. Rabaey - Univ. of California, Berkeley, CA

James A. Rowson - Alta Group of Cadence Design Systems, Inc., Sunnyvale, CA

Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

Audience: This tutorial is intended for engineers and managers involved directly in design or in CAD who want to gain a perspective on the critical issues regarding emerging tools to support system-level design.

Description: System design issues are gaining more and more importance as time-to-market shrinks and complexity rises. Isolated attempts have been made to address portions of the system design problem, but a more holistic approach is needed. The relatively independent approaches need to be related and the critical links to current implementation approaches for both hardware and software need to be created.

Industry is now clamoring for tools to help system designers evaluate at ever higher levels of abstraction to permit more effective exploration of the design space and the tradeoffs between functionality and implementation constraints. Moreover, there is a corresponding need for increased automation in generating many of the details of a system implementation so that designs can be more quickly prototyped and produced. A fundamental part of this is realizing the promise of design reuse and facilitating the growth of a market for intellectual property in both embedded hardware and software. There are four principal elements to realizing the vision of system-level tools: modeling and abstraction, software and hardware reuse, estimation and evaluation, synthesis and compilation. In this tutorial, we will review these issues and highlight some promising directions with some examples of the types of tools that are emerging.

Tutorial
FourInterconnect Analysis in High-Frequency,
Sub-Micron, Digital VLSI Design

Room 304

Organizer: *Peter Feldmann* - Lucent Technologies Bell Labs., Murray Hill, NJ

Presenters:

Peter Feldmann - Lucent Technologies Bell Labs., Murray Hill, NJ

Roland W. Freund - Lucent Technologies Bell Labs., Murray Hill, NJ

Tak Young - Synopsys, Inc., Mountain View, CA

Audience: This tutorial is intended for CAD tool developers and researchers, for engineers responsible for design methodologies, and for VLSI designers who need to understand the capabilities and limitations of the tools they use.

Description: This tutorial focuses on the principal problems related to interconnect-parasitics extraction and analysis in advanced, high-frequency, digital VLSI applications. First, we review the parasitic effects of interconnect: capacitance, resistance, inductance, transmission-line effects, and substrate noise. We discuss when the various interconnect aspects become important, when some of them can be safely ignored, and future trends.

Next, we discuss the various extraction approaches and their domains of applicability. We cover the entire spectrum from simple capacitance to resistance-capacitance extraction, to full-wave analysis. We describe specific techniques, including formula-based approaches, 2D analysis, 2 1/2D analysis, 3D methods, the use of field solvers such as finite elements and the method of moments, and fast algorithms such as multiple techniques.

The next challenging task then is to handle the enormous amount of data generated by extraction at the chip level. This requires smart screening techniques, efficient data reduction, and fast and accurate simulation. We cover these techniques in the context of two important interconnect-analysis problems: verification against cross-talk and reliability analysis. For the analysis and reduction of the interconnect models, Krylov-subspace techniques have emerged as the methods of choice. These methods generate reduced-order models based on Pade or Pade-type approximations of the frequency-domain transfer function. We survey the state-of-the-art in Krylov-subspace methods for interconnect analysis. In particular, we discuss important issues, such as accuracy, stability, and passivity of the reduced-order models.

Finally, we illustrate the incorporation of interconnect extraction and analysis in the VLSI design flow with two examples: transistor-level design and cell-based design. Here, the design flows include signal screening, critical-path selection, and delay calculation. The inclusion of interconnect-parasitics effects in clock-skew analysis, power calculation, in cross-talk analysis, and in reliability simulation will also be discussed.

Tutorial
FiveFinding Design Errors and Locating Defects: Room 301
The Same Detective Story

Organizer: *Miron Abramovici* - Lucent Technologies Bell Labs., Murray Hill, NJ

Presenters:

Miron Abramovici - Lucent Technologies Bell Labs., Murray Hill, NJ

Robert Aitken - Hewlett-Packard, Palo Alto, CA

Audience: Designers, researchers, managers, and anyone determined to find out where those puzzling errors are coming from.

Suggested Prerequisites: Logic and circuit design, basic testing concepts, and a strong desire to discover if indeed the butler did it.

Description: Locating design errors is a key factor in the logic verification process. Errors can result from incorrect specifications, erroneous logic implementation, and/or timing problems. Just as accurate error location is needed to meet time-to-market goals, accurate physical defect location is essential in improving the quality of the manufacturing process, and rapid identification of a defective replaceable part is essential in achieving a cost-effective field maintenance and repair process. The efficiency of all forms of diagnosis has a great economic impact on the cost of a product during its entire life-cycle (cost-of-ownership). Unlike fault and defect diagnosis, the practice of logic debugging is more of an engineering art than a science, and tools for diagnosis in the logic domain are still in experimental/prototype stage.

The tutorial will present methods for finding design implementation errors and techniques for locating defects in circuits. We will point out the many similarities between logical and physical diagnosis, and we will emphasize the common principles that guide each diagnosis process. After a review of the basic concepts in diagnosis, we will present the established defect diagnosis procedures - fault dictionary, post-test fault simulation, and guided-probe/E-beam testing. Then we will focus on advanced diagnosis topics such as critical path tracing, deductive analysis, diagnosis for delay-faults, AI techniques, and methods for locating defects such as opens, shorts, and leakage in transistor-level circuits.

In the logic domain, we will present several techniques to automatically generate design verification tests, and several methods that locate the logic error(s) that cause mismatches between implementation and specification. We will also discuss techniques that automatically correct the located errors. The models where errors are located range from VHDL to transistor-level designs. In addition to logic errors, we will discuss techniques to locate timing problems in circuits, and discuss design-for-debug methods to simplify this process.

Tutorial
SixHigh Performance RTL Coding
Styles for Synthesis

Room 306

Organizer: *Joseph Pick* - Synopsys, Inc., Bethesda, MD

Presenters:

J. Bhasker - Lucent Technologies Bell Labs., Allentown, PA

Egbert Molenkamp - Univ. of Twente, Enschede, The Netherlands

Joseph Pick - Synopsys, Inc., Bethesda, MD

Audience: This tutorial is intended for current and future synthesis users who wish to accumulate a collection of coding style tricks and techniques that will improve their overall synthesis productivity. A basic understanding of either the VHDL or Verilog hardware description language is assumed.

Description: Having attended an introductory VHDL or Verilog simulation based class digital designers must then subsequently, by themselves, discover the interplay and duality between software coding styles and their hardware counterparts as derived via synthesis. These engineers must, on their own, rapidly master the fundamentals of synthesizable RTL coding styles and then, through trial and error, explore the best way to write their VHDL/Verilog models so that they will have optimum synthesis results. This steep and often lonely learning curve can be a very frustrating experience, especially when a project deadline is just a few months away.

Lack of education in the area of coding styles for RTL synthesis will have a negative impact on an engineer's overall productivity. The main thrust of this tutorial is to overcome many of these design barriers by spanning the full spectrum of synthesis RTL coding styles, from fundamental principles to advanced techniques. This innovative, examples oriented tutorial will be an educational and entertaining experience for both current and future synthesis users. The first half of this tutorial will present numerous real-world examples from the following topics: synthesizable and non-synthesizable VHDL/Verilog constructs, duality between VHDL/Verilog models and synthesized hardware, importance of VHDL/Verilog coding styles for efficient hardware synthesis, simulation and synthesis mismatches, relying on hardware design experiences, and advanced VHDL/Verilog strategies and techniques. The second half of this tutorial will present a detailed exploration of FSMs and test benches. The migration path from device specification to synthesizable code will be shown for numerous, complex devices. Experiencing the derivation of these complex, synthesizable models will further improve the productivity of synthesis users.