



9:00 to 10:15

General Session and Keynote Speaker (no badge is required)
March of Technology

Paul Otellini - Executive Vice President, Intel, Corp., Santa Clara, CA
Opening Remarks • Awards • Keynote Address • (Main Auditorium)

Break

BREAK

RM #

Table with 5 columns: RM 273, RM 288, RM 291, RM 293, Auditorium B. Rows include Session 1-5 and session topics like Advances in Model Reduction, Combinatorial Problems, IP-Based Design, Low-Power Design, and Panel: HW and SW in Embedded System Design.

Lunch

LUNCH 12:00 - 2:00

RM #

Table with 5 columns: RM 291, RM 293, Auditorium A, Auditorium C, Auditorium B. Rows include Session 6-10 and session topics like Routing for Deep Submicron, Asynchronous Logic Synthesis, System-Level Power Optimization, Networked Embedded Systems, and Functional Verification of Microprocessors.

Break

BREAK

4:30 to 6:00

Table with 5 columns: Session 11, Session 12, Session 13, Session 14, Session 15. Topics include Interconnect and Passive Component Modeling, New Concepts in Behavioral and Logic Synthesis, Performance and Power Optimization, Software Driven Architecture, and Panel: Functional Verification: Real Users, Real Problems, Real Opportunities.

6:00 to 7:00

DAC Cocktail Party at the Ernest N. Morial Convention Center
6:00PM - 7:00PM in the La Nouvelle Orleans Ballroom Section C

Exhibit Hours 10:00AM-6:00PM / Demo Suite Hours 8:00AM-9:00PM

All Design Methods Sessions are shaded purple, Embedded Systems Sessions are shaded grey.



RM #	RM 291	RM 293	Auditorium A	Auditorium C	Auditorium B
	Session 16	Session 17	Session 18	Session 19	Session 20
8:30 to 10:00	Floorplanning	Scheduling Algorithms for High Level Synthesis	Symbolic Model Checking	DSP Design Techniques and Implementations	Panel: Cell Libraries Build vs. Buy, Static vs. Dynamic
Break	BREAK				
	Session 21	Session 22	Session 23	Session 24	Session 25
10:30 to 12:00	Partitioning and Linear Placement	Technology Dependent Synthesis and Optimization	Advances in Symbolic Simulation	System Level Design Methodology and Case Studies	Panel: Parasitic Extraction Accuracy: How Much Is Enough?
Lunch	LUNCH 12:00 - 2:00				
	Session 26	Session 27	Session 28	Session 29	Session 30
2:00 to 4:00	Circuit Optimization for Power and Performance	Interaction of Synthesis and Layout	Interconnect Issues for Deep-Submicron Design	Design Entry and Specification	Panel: MEMS CAD: Beyond Multi-Million Transistors
Break	BREAK				
	Session 31	Session 32	Session 33	Session 34	Session 35
4:30 to 6:00	Extraction of Capacitance and Substrate Models	High-Level Techniques for Low Power	System-Level Verification and Test	Logic and High-Level Synthesis Methodologies	Reconfigurable Systems
36th Dac Party 7:30PM - 10:00PM at the New Orleans Hilton Riverside					

Exhibit Hours 10:00AM–6:00PM / Demo Suite Hours 8:00AM–9:00PM



RM #	RM 291	RM 293	Auditorium A	Auditorium C	Auditorium B
	Session 36	Session 37	Session 38	Session 39	Session 40
8:30 to 10:00	RF Simulation	Advanced Test Generation and Diagnosis	RTL Circuit Simulation	CAD Solutions Using FPGAs	Technology Directions
Break	BREAK				
	Session 41	Session 42	Session 43	Session 44	Session 45
10:30 to 12:00	Timing Analysis and Optimization	Built-In Self-Test Solutions	Clock, Power Distribution and Analog Issues	Modeling for Design Reuse	Panel: Sub-Wavelength Lithography: How Will It Impact Your Design Flow?
12:00 Lunch 2:00	KEYNOTE 1:00 - 1:45 (Lunch Not Included) <i>EDA to the Rescue of System on a Chip</i> Aart de Geus - Chair, EDA Consortium & CEO, Synopsys, Inc., Mountain View, CA Auditorium B (no badge is required)				
	Session 46	Session 47	Session 48	Session 49	Session 50
2:00 to 4:00	Software Implementation for DSP Applications	Intellectual Property Protection Using Watermarking	Low Power System Design Techniques	Emerging Directions	Inductance Issues In High Frequency Design
Break	BREAK				
	Session 51	Session 52	Session 53	Session 54	Session 55
4:30 to 6:00	Instruction-Level ASIP Design	Analog Synthesis and Modeling	Simulation and Test	Designing On-Chip Inductors	Panel: What is the Proper SOC Design Methodology?

Demo Suite Hours 8:00AM–5:00PM

Tutorials will be held at the Ernest N. Morial Convention Center in the 2nd level meeting rooms.

8:00 AM - Tutorial Registration Opens (Esplanade Lobby)

12:00 - 1:00 - Lunch

8:30 AM - Continental Breakfast

5:00 PM - Tutorials End

9:00 AM - Tutorials Begin

Tutorial 1**Rooms 286-287****Automated Layout and Migration in Ultra-Deep Submicron VLSI**

Organizer: *Andrew B. Kahng* - Univ. of California, Los Angeles, CA

Tutorial 2**Rooms 291-292****Analog and Mixed-Signal Modeling Using the VHDL-AMS Language**

Organizer: *Ernst Christen* - Analogy, Inc., Beaverton, OR

Tutorial 3**Rooms 293-294****Information Visualization: Creating Advanced Visual Interfaces for Analyzing Designs**

Organizer: *Eric Solomon* - Synopsys, Inc., Mountain View, CA

Tutorial 4**Rooms 295-296****Overcoming the Technical and Managerial Challenges in Enabling Design Reuse Within the Engineering Organization**

Organizer: *Mike Keating* - Synopsys, Inc., Mountain View, CA

Tutorial 5**Rooms 298-299****Embedded Memories in System Design - From Technology to Systems Architecture**

Organizer: *Francky Catthoor* - IMEC, Leuven, Belgium

Tutorial 6**Rooms 289-290****Built-In Self-Test for Systems on a Chip**

Organizer: *Janusz Rajski* - Mentor Graphics Corp., Wilsonville, OR

If you are interested in the following topics please see the related sessions listed below.

Please be advised that the two Keynotes and some of the Technical Sessions will be video taped during the conference.

Embedded Systems

Sessions: 5, 8, 9, 14, 44, 46, Tutorial 5

System Design and Optimization

Sessions: 3, 19, 24, 29, 33, 46, 51, Tutorial 5

Logic and High Level Synthesis and Optimization

Sessions: 7, 12, 17, 22, 27, 34

Logic and Functional Verification and Simulation

Sessions: 10, 15, 18, 23, 38, Tutorial 3

Electrical Modeling and Simulation

Sessions: 1, 25, 36, 41, Tutorial 3

Physical Design

Sessions: 6, 16, 20, 21, 27, 43, Tutorial 1

Validation and Test

Sessions: 33, 37, 38, 42, 53, Tutorial 6

Impacts of Advancing Technology

Sessions: 28, 30, 35, 39, 40, 45, 49, Tutorial 1

Device and Interconnect Modeling

Sessions: 11, 25, 28, 31, 49, 50

Analog and Mixed Signal Design

Sessions: 36, 43, 52, 54, Tutorial 2

Low Power Design

Sessions: 4, 8, 13, 26, 32, 48

Design Reuse, IP and SoC Issues

Sessions: 3, 44, 47, 55, Tutorial 4, Tutorial 6



Tuesday, June 22

opening session

9:00 AM
to
10:15 AM
Auditorium



opening remarks

Mary Jane Irwin
General Chair

Randal E. Bryant
Design Tools Co-Chair

Bryan Ackland
Design Methods Co-Chair

awards presented by:

Steven P. Levitan
ACM Representative

Michael Lightner
IEEE/CAS Representative

opening keynote address

Paul Otellini
Executive Vice President
Intel Corp., Santa Clara, CA

awards/scholarships

ASCEE undergraduate scholarships

Scholarships will be awarded to three high school students who will be pursuing a degree in Electrical Engineering or Computer Science from under-represented minorities.

graduate scholarships

Scholarships will be awarded to four graduate students to support research in Design Automation.

individual awards

1999 IEEE Fellow Awards

ACM Kanellakis Award

IEEE Transaction on CAD Best Paper

IEEE Transaction on VLSI Best Paper

1999 SIGDA Distinguished Service Awards

1999 SIGDA Doctoral Thesis Awards

design contest winners

The three finalists are featured in the Technical Program in sessions 19 and 48.

best paper awards

Best Paper Awards will be given in the following areas:

1. **Physical and Electrical Design Modeling and Estimation**
2. **Logic-Level Testing, Simulation and Synthesis**
3. **High-Level Synthesis Verification and Co-Design**
4. **System Level Design Methodology**
5. **Technology Driven Design Methodology**

**All Design Methods Sessions are shaded purple.
All Embedded Systems Sessions are shaded grey.**

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uesday, june 22

technical
program10:30
to
12:00§ - denotes
best paperAll speakers are
denoted in **bold**S - denotes
short paper
presentation,
15 minutes**SESSION 1****ROOM:** 273**ADVANCES IN MODEL
REDUCTION****Chair:** *Joel R. Phillips* - Cadence Design
Systems, Inc., San Jose, CA**Organizers:** *Hidetoshi Onodera, Joel R. Phillips*

This session features recent advances in model-reduction algorithms. The first paper uses methods similar to the popular Krylov-subspace and moment-matching techniques, but produces much better approximations. The second paper presents a method for rational approximation with bounded error in the time-domain. The third contribution proposes model reduction algorithms for nonlinear circuits, and the fourth shows how to exploit symmetry in reduction of RLC circuits.

1.1 An Efficient Lyapunov Equation-Based Approach for Generating Reduced-Order Models of Interconnect***Jing-Rebecca Li***, *Frank Wang, Jacob K. White* - Massachusetts Institute of Technology, Cambridge, MA**1.2 Error Bounded Pade Approximation via Bilinear Conformal Transformation*****Chung-Ping Chen*** - Intel Corp., Hillsboro, OR
Martin D.F. Wong - Univ. of Texas, Austin, TX**1.3S Model-Reduction of Nonlinear Circuits Using Krylov-Space Techniques*****Pavan Gunupudi***, *Michel Nakhla* - Carleton Univ., Ottawa, Canada**1.4S ENOR: Model Order Reduction of RLC Circuits Using Nodal Equations for Efficient Factorization*****Bernard N. Sheehan*** - Mentor Graphics Corp., Wilsonville, OR**SESSION 2****ROOM:** 288**COMBINATORIAL PROBLEMS****Chair:** *Fabio Somenzi* - Univ. of Colorado, Boulder, CO**Organizers:** *Sharad Malik, Andrew B. Kahng*

This session focuses on key combinatorial analysis problems that potentially span multiple application areas in EDA. The problem areas covered are ATPG, BDDS, SAT and Cycle Mean Computation for graphs.

2.1 Why Is ATPG Easy?***Mukul R. Prasad***, *Philip Chong, Kurt Keutzer* - Univ. of California, Berkeley, CA**2.2S Using Lower Bounds During Dynamic BDD Minimization*****Rolf Drechsler***, *Wolfgang Günther* - Univ. of Freiburg, Freiburg, Germany**2.3S Optimization-Intensive Watermarking Techniques for Decision Problems*****Gang Qu***, *Jennifer L. Wong, Miodrag Potkonjak* - Univ. of California, Los Angeles, CA**2.4 Efficient Algorithms for Optimum Cycle Mean and Optimum Cost to Time Ratio Problems*****Ali Dasdan*** - Univ. of Illinois, Urbana, IL
Sandra Irani, Rajesh K. Gupta - Univ. of California, Irvine, CA



SESSION 3

ROOM: 291

IP-BASED DESIGN

Chair: *David Ku* - Escalade Corp., Santa Clara, CA

Organizers: *Rajesh K. Gupta, David Ku*

This session focuses on approaches to IP-Based design, starting with an invited talk outlining the issues and challenges in IP-Driven design methodology. Following the overview, the first paper describes an integrated system for distributed embedded system design. The second paper describes an approach to virtual simulation of distributed, Java-based IP models.

3.1 INVITED PAPER: IP-Based Design Methodology

Daniel D. Gajski - Univ. of California, Irvine, CA

3.2 IPCHINOOK: An Integrated IP-Based Design Framework for Distributed Embedded Systems

Pai Chou, Ross B. Ortega, Ken Hines, Kurt Partridge, Gaetano Borriello - Univ. of Washington, Seattle, WA

3.3 Virtual Simulation of Distributed IP-Based Designs

Marcello Dalpasso - Univ. of Padova, Padova, Italy

Alessandro Bogliolo, Luca Benini - Univ. of Bologna, Bologna, Italy

SESSION 4

ROOM: 293

LOW-POWER DESIGN USING VOLTAGE SCALING

Chair: *Tadahiro Kuroda* - Toshiba Corp., Kawasaki, Japan

Organizers: *Anantha Chandrakasan, Mojoy Chian*

This session presents low-power design methodologies and techniques using voltage scaling. The first paper proposes a design technique that identifies and optimizes frequently-encountered behavioral computations. The next three papers address the use of multiple supplies to reduce power by assigning lower voltages to non-critical paths. Synthesis and layout techniques for dual supplies are reported.

§4.1 Common Case Computation: A High-Level Technique for Power and Performance Optimization

Ganesh Lakshminarayana, Anand Raghunathan - NEC USA, Princeton, NJ
Kamal S. Khouri, Niraj K. Jha - Princeton Univ., Princeton, NJ

Sujit Dey - Univ. of California at San Diego, La Jolla, CA

4.2 Layout Techniques Supporting the Use of Dual Supply Voltages

Chingwei Yeh, Yin-Shuin Kang, Jinn-Shyan Wang, Shan-Jih Shieh - National Chung-Cheng Univ., Chiayi, Taiwan ROC

4.3S Gate-Level Design Exploiting Dual Supply Voltages for Power-Driven Applications

Chingwei Yeh, Min-Cheng Chang, Shih-Chieh Chang, Wen-Bone Jone - National Chung-Cheng Univ., Chiayi, Taiwan ROC

4.4S Synthesis of Low Power CMOS VLSI Circuits Using Dual Supply Voltages

Vijay Sundararajan, Keshab K. Parhi - Univ. of Minnesota, Minneapolis, MN

SESSION 5

ROOM: AUDITORIUM B

EMBEDDED SYSTEMS PANEL: HW AND SW IN EMBEDDED SYSTEM DESIGN: LOVEBOAT, SHIPWRECK, OR SHIPS PASSING IN THE NIGHT

Chair: *Kurt Keutzer* - Univ. of California, Berkeley, CA

Organizers: *Raul Camposano, Kurt Keutzer*

The merging of hardware and software in a single integrated circuit is causing many to rethink their approach to embedded system design, and many are forecasting significant changes in the associated electronic-design automation and embedded software industries as well. For some, the ocean of silicon ahead is sure to host a loveboat for fully integrated hardware/software systems. Others see a shipwreck on the horizon, as hard-headed hardware designers and soft-headed software developers clash at sea. Still others predict that as severe power constraints cause hardware-designers to eschew software solutions, and as the world of ubiquitous computing significantly broadens the market for embedded system software, then the hardware and software communities will be simply ships passing in the night.

PANEL MEMBERS:

Raul Camposano - Synopsys, Inc., Mountain View, CA

Jerry L. Fiddler - Wind River Systems, Alameda, CA

Joseph Fisher - Hewlett-Packard Co., Cambridge, MA

Kurt Keutzer - Univ. of California, Berkeley, CA

Jim Lansford - Intel Corp., Stillwater, OK

Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA



2:00
to
4:00§ - denotes
best paper**SESSION 6****ROOM:** 291**ROUTING FOR DEEP
SUBMICRON****Chair:** *Patrick Groeneveld* - Magma Design
Automation, Inc., Cupertino, CA**Organizers:** *Patrick Groeneveld, Lou Scheffer*

This session addresses relevant problems in deep-submicron routing. The first paper presents a powerful optimization method for power routing. The second and third papers deal with wire and driver sizing under various constraints. The last two papers provide practical solutions for DSM signal integrity problems.

**§6.1 Area Optimization of VLSI Power/Ground
Networks Via Sequence of Linear Programmings**

Xiangdong Tan, *C.J. Richard Shi, Dragos Lungeanu* - Univ. of Washington, Seattle, WA
Jyh-Chwen Frank Lee, Li-Pen Yuan - Avant! Corp., Fremont, CA

**6.2 FAR-DS: Full-Plane Awe Routing with Driver
Sizing**

Jiang Hu, *Sachin S. Sapatnekar* - Univ. of Minnesota, Minneapolis, MN

**6.3 Noise-Constrained Performance
Optimization By Simultaneous Gate and Wire
Sizing Based on Lagrangian Relaxation**

Hui-Ru Jiang, *Jing-Yang Jou, Yao-Wen Chang* - National Chiao Tung Univ., Hsinchu, Taiwan ROC

**6.4S Simultaneous Routing and Buffer Insertion
With Restrictions on Buffer Locations**

Hai Zhou, *Martin D. F. Wong, I-Min Liu, Adnan Aziz* - Univ. of Texas, Austin, TX

**6.5S Crosstalk Minimization Using Wire
Perturbations**

Prashant Saxena - Intel Corp., Hillsboro, OR
C.L. Liu - National Tsing Hua Univ., Hsin Chu, Taiwan ROC

SESSION 7**ROOM:** 293**ASYNCHRONOUS LOGIC
SYNTHESIS****Chair:** *Prabhakar Kudva* - IBM Corp., Yorktown Heights, NY**Organizers:** *Timothy Y. Kam, Luciano Lavagno*

This session presents an overview of the state of the art in asynchronous circuit synthesis and analysis. The initial embedded tutorial is devoted to a complete design methodology for asynchronous controllers, based on concurrent finite state machines operating in fundamental mode. The second talk describes synthesis techniques from a high-level channel-based specification to a lower-level event-based synthesizable specification. The third talk describes a probabilistic technique for performance analysis of asynchronous timing diagram-like specifications. The last presentation from Intel Strategic CAD Lab., describes a high performance low power asynchronous instruction decoder.

**7.1 EMBEDDED TUTORIAL: Practical Advances
in Asynchronous Design and
Asynchronous/Synchronous Interfaces**

Steven M. Nowick - Columbia Univ., New York, NY
Erik Brunvard - Univ. of Utah, Salt Lake City, UT
Kenneth Yun - Univ. of California, San Diego, CA
(1hr. 15 min. presentation)

**7.2S Automatic Synthesis and Optimization of
Partially Specified Asynchronous Systems**

Alex Kondratyev - Univ. of Aizu, Fukushima, Japan
Jordi Cortadella - Univ. Politecnica de Catalunya, Barcelona, Spain
Michael Kishinevsky - Intel Corp., Hillsboro, OR
Luciano Lavagno - Politecnico di Torino, Torino, Italy
Alexandre Yakovlev - Univ. of Newcastle Upon Tyne, Newcastle Upon Tyne, UK

**7.3 INVITED PAPER: CAD Requirements for
High Performance Asynchronous Circuits**

Shai Rotem, Ken Stevens, M. Kishinevsky, R. Ginosar, S. Burns, M. Roncken - Intel Corp., Hillsboro, OR



SESSION 8

ROOM: AUDITORIUM A

SYSTEM-LEVEL POWER OPTIMIZATION

Chair: *Rajesh K. Gupta* - Univ. of California, Irvine, CA

Organizers: *David Ku, Rajesh K. Gupta*

System level power optimization is attractive for its scope and effectiveness. Papers in this session deal with partitioning and task scheduling and design of components such as memory and interfaces to reduce power.

8.1 A Low Power Hardware/Software Partitioning Approach for Core-Based Embedded Systems

Joerg Henkel - NEC USA, C&C Research Labs., Princeton, NJ

8.2 Synthesis of Low-Overhead Interfaces for Power-Efficient Communication Over Wide Buses

Luca Benini - Univ. of Bologna, Bologna, Italy

Alberto Macii, Enrico Macii, Massimo Poncino, Riccardo Scarsi - Politecnico di Torino, Torino, Italy

8.3 Power Conscious Fixed Priority Scheduling for Hard Real-Time Systems

Youngsoo Shin, Kiyoung Choi - Seoul National Univ., Seoul, Korea

8.4 Memory Exploration for Low Power, Embedded Systems

Chaitali Chakrabarti, Wen-Tsong Shiue - Arizona State Univ., Tempe, AZ

SESSION 9

ROOM: AUDITORIUM C

NETWORKED EMBEDDED SYSTEMS: OS, MIDDLEWARE, AND PROTOCOLS

Chair: *Asawaree Kalavade* - Bell Labs., Lucent Technologies, Murray Hill, NJ

Organizers: *Raul Camposano, Asawaree Kalavade, Sharad Malik, James Rowson, Patrick Scaglia*

With the growing demands of ubiquitous information access, consumer applications are increasingly required to be networked. Understanding the characteristics and constraints of these applications and the underlying technologies that support them is key to solving design problems in next-generation 'networked' embedded systems. This session focuses on some emerging technologies in this context.

The first two talks describe the role of the operating system in supporting high-performance real-time applications. The third talk describes a middleware technology that allows applications to communicate seamlessly across a distributed network. The last talk describes the networking protocols used to connect such embedded systems within the home.

9.1 INVITED PAPER: Distributed Application Development with Inferno

Ravi Sharma - INS Solutions, Lucent Technologies, Freehold, NJ

9.2 INVITED PAPER: Embedded Application Design Using a Real-Time OS

David Stegner - Integrated Systems, Inc., Sunnyvale, CA

9.3 INVITED PAPER: The Jini Architecture: Dynamic Services in a Flexible Network

Ken Arnold - Sun Microsystems, Inc., Burlington, MA

9.4 INVITED PAPER: Networking the Home - Wireless Technologies and Protocols

Paramvir Bahl - Microsoft Research, Redmond, WA

SESSION 10

ROOM: AUDITORIUM B

FUNCTIONAL VERIFICATION OF MICROPROCESSORS

Chair: *Rajesh Raina* - Motorola, Inc., Austin, TX

Organizers: *Rajesh Raina, Vivek Tiwari*

Verification of large systems continues to be a challenge. This session presents practiced verification experiences from commercial microprocessor efforts. A diverse set of verification methodologies, including an abstract verification environment and various test generation strategies, are presented.

10.1 Verifying Large-Scale Multiprocessors Using an Abstract Verification Environment

Dennis Abts, Mike Roberts - Silicon Graphics, Inc., Chippewa Falls, WI

10.2 Functional Verification of the Equator Map1000 Microprocessor

Jian Shen, Jacob A. Abraham - Univ. of Texas, Austin, TX

Dave Baker, Tony Hurson, Martin Kinkade, Gregoria Gervasio, Chen-Chau Chu, Guanghui Hu - Equator Technologies Inc., Austin, TX

10.3S Micro Architecture Coverage Directed Generation of Test Programs

Shmuel Ur, Yoav Yadin - IBM Corp., Haifa, Israel

10.4S Verification of A Microprocessor Using Real World Applications

You-Sung Chang, Seungjong Lee, In-Cheol Park, Chong-Min Kyung - KAIST, Taejeon, Korea

10.5S High-Level Test Generation for Design Verification of Pipelined Microprocessors

David Van Campenhout, Trevor Mudge, John P. Hayes - Univ. of Michigan, Ann Arbor, MI

10.6S Developing An Architecture Validation Suite - Application To The PowerPC Architecture

Laurent Fournier, Anatoly Koyfman, Moshe Levinger - IBM Corp., Haifa, Israel

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uesday, june 22

technical
program4:30
to
6:00**SESSION 11****ROOM:** 291**INTERCONNECT AND
PASSIVE COMPONENT
MODELING****Chair:** *Alan Mantooth* - Univ. of Arkansas,
Fayetteville, AR**Organizers:** *Hidetoshi Onodera, Alan Mantooth*

The first two papers in this session are devoted to model order reduction for interconnect. The first paper describes a nice preview of reduced-order modeling along with its description of a projection technique based on Krylov subspaces for this purpose. The second paper combines matrix perturbation, dominant-pole analysis and Krylov subspaces to produce reduced order models including manufacturing variations. The last paper is a new method of function approximation where a state space model is derived from tabular frequency domain data for linear model generation.

11.1 Passive Reduced-Order Models for Interconnect Simulation and their Computation Via Krylov-Subspace Algorithms**Roland W. Freund** - Lucent Technologies, Bell Labs., Murray Hill, NJ**11.2 Model Order-Reduction of RC(L) Interconnect Including Variational Analysis****Ying Liu, Lawrence T. Pileggi, Andrzej J. Strojwas** - Carnegie Mellon Univ., Pittsburgh, PA**11.3 Robust Rational Function Approximation Algorithm for Model Generation****Carlos Coelho** - Technical Univ. Lisbon, Lisbon, Portugal**Joel R. Phillips** - Cadence Design Systems, Inc., San Jose, CA**L. Miguel Silveira** - Technical Univ. of Lisbon, Lisbon, Portugal**SESSION 12****ROOM:** 293**NEW CONCEPTS IN
BEHAVIORAL AND LOGIC
SYNTHESIS****Chair:** *Timothy Y. Kam* - Intel Corp., Hillsboro, OR**Organizers:** *Kazutoshi Wakabayashi,
Timothy Y. Kam*

This session is devoted to new ideas in high-level and logic synthesis. The first paper introduces a novel internal model for high-level synthesis inspired by the logic network, that helps to bridge the gap between the two synthesis domains. The second paper presents a flexible scheduling framework called soft scheduling where less critical scheduling decisions can be deferred and adjusted later. The third paper is on functional decomposition through graph coloring for the column multiplicity problem.

12.1 Behavioral Network Graph: Unifying the Domains of High-Level and Logic Synthesis**Reinaldo Bergamaschi** - IBM Corp., Yorktown Heights, NY**12.2 Soft Scheduling In High Level Synthesis****Jianwen Zhu, Daniel D. Gajski** - Univ. of California, Irvine, CA**12.3 Graph Coloring Algorithms for Fast Evaluation of Curtis Decompositions****Marek A. Perkowski, Rahul Malvi, Stanislaw Grygiel, Mike Burns, Alan Mishchenko** - Portland State Univ., Portland, OR



SESSION 13

ROOM: AUDITORIUM A

PERFORMANCE AND POWER OPTIMIZATION

Chair: *Narendra V. Shenoy* - Synopsys, Inc., Mountain View, CA

Organizers: *Timothy Y. Kam, Luciano Lavagno*

Retiming has been proven as a practically useful performance optimization tool. This session presents research advances in retiming. The first paper proposes exact and heuristic optimization by simultaneous application of retiming and clock skew scheduling. The second paper extends retiming to handle complex registers. The third paper couples retiming and resynthesis to meet performance targets. Power optimization is the focus of the fourth paper which is based on the extraction of the computationed kernel from an STG.

13.1 Maximizing Performance by Retiming and Clock Skew Scheduling

Marios C. Papaefthymiou - Univ. of Michigan, Ann Arbor, MI

Eby G. Friedman - Univ. of Rochester, Rochester, NY

Xun Liu - Univ. of Michigan, Ann Arbor, MI

13.2 A Practical Approach to Multiple-Class Retiming

Klaus Eckl - Technical Univ. of Munich, Munich, Germany

Jean Christophe Madre - Synopsys, Inc., Gieres, France

Peter W. Zepher - Synopsys, Inc., Mountain View, CA

Christian Legl - Technical Univ. of Munich, Munich, Germany

13.3S Performance-Driven Integration of Retiming and Resynthesis

Peichen Pan - Intel Corp., Hillsboro, OR

13.4S Kernel-Based Power Optimization of RTL Components: Exact and Approximate Extraction Algorithms

Luca Benini - Univ. of Bologna, Bologna, Italy

Giovanni De Micheli - Stanford Univ., Stanford, CA

Enrico Macii, Giuseppe Odasso, Massimo

Poncino - Politecnico di Torino, Torino, Italy

SESSION 14

ROOM: AUDITORIUM C

SOFTWARE DRIVEN ARCHITECTURE

Chair: *Patrick Scaglia* - Cadence Labs., San Jose, CA

Organizers: *Raul Compasano, Asawaree Kalavade, Sharad Malik, James Rowson, Patrick Scaglia*

With the proliferation of embedded computing in almost every aspect of our life, the demand on the creation of extremely powerful, yet low cost processing systems is escalating. The notion of special purpose computing is being redefined, and with it, new approaches in Architecture and Compiler technologies. This session focuses on some emerging technologies in this context.

The first talk will argue that the pressure towards standardization of architectures will soon be going in the reverse direction: we will eventually see far greater specialization of embedded architectures for specific use. In the second talk, the author observes that great system-level solutions come from cooperating innovations between software and hardware designers, who keep the total system foremost in their mind. The third talk will cover the latest contribution for the development of DSP software.

14.1 INVITED PAPER: Customized Instruction-Sets for Embedded Processors

Joseph A. Fisher - Hewlett-Packard Co., Cambridge, MA

14.2 INVITED PAPER: A System-Level View of Hardware/Software Tradeoffs

Samuel P. Harbison - Texas Instruments, Monroeville, PA

14.3 INVITED PAPER: Next-Generation DSP Software Development Tools

Paul G. D'Arcy - Lucent Technologies, Atlanta, GA

SESSION 15

ROOM: AUDITORIUM B

PANEL: FUNCTIONAL VERIFICATION: REAL USERS, REAL PROBLEMS, REAL OPPORTUNITIES

Chair: *John McLeod* - Silicon Strategies, Mountain View, CA

Organizers: *Ghulam Nurie, Mike Murray*

Achieving timely and comprehensive functional design verification is a ubiquitous problem in electronics. This panel presents designers of cardiac pacemakers, communications satellites, computer servers, networking equipment, and IP discussing verification.

The panelists will begin by dissecting the bottlenecks in their verification processes. For example, are simulators too slow? Or do test vector generation and coverage analysis consume the most time? The panelists will present their ideas for new EDA products which might accelerate verification. Finally, the panelists will discuss what compromises they would accept in order to achieve this acceleration. Would they learn a new HDL? Restrict their design styles? Forsake legacy designs?

This panel will be of interest to both EDA users and developers.

PANEL MEMBERS:

Nozar Azarakhsh - Cisco Systems, Inc., San Jose, CA

Glen Ewing - Hughs Space and Communications Co., El Segundo, CA

Paul Gingras - Sun Microsystems, Inc., Burlington, MA

Scott Reedstrom - Guidant Corp., St. Paul, MN

Chris Rowen - Tensilica, Inc., Santa Clara, CA





8:30
to
10:00

§ - denotes best paper

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SESSION 16

ROOM: 291

FLOORPLANNING

Chair: *Louis Scheffer* - Cadence Design Systems, Inc., San Jose, CA

Organizers: *Louis Scheffer, Patrick Groeneveld*

This session concentrates on floorplanning and its interaction with other tools in the design flow. The first paper improves the interaction between floorplanning, synthesis, and physical implementation tools. The second introduces a new representation for floorplanning and the third extends techniques developed for floorplanning to do analog placement.

16.1 A Timing-Driven Soft-Macro Resynthesis Method in Interaction with Chip Floorplanning

Hsiao-Pin Su - Tsing Hua Univ./Taiwan Semiconductor Manufacturing Co. Ltd., Hsinchu, Taiwan ROC

Allen C.H. Wu, Youn-Long Lin - Tsing Hua Univ., Hsinchu, Taiwan ROC

16.2 An O-Tree Representation of Non-Slicing Floorplan and Its Applications

Pei-Ning Guo, Chung-Kuan Cheng - Mentor Graphics, Corp., San Jose, CA
Takeshi Yoshimura - NEC Corp., Kawasaki, Japan

16.3 Module Placement for Analog Layout Using The Sequence-Pair Representation

Florin Balasa, Koen Lampaert - Conexant Systems, Newport Beach, CA

SESSION 17

ROOM: 293

SCHEDULING ALGORITHMS FOR HIGH LEVEL SYNTHESIS

Chair: *Kazutoshi Wakabayashi* - NEC Corp., Kawasaki, Japan

Organizers: *Timothy Y. Kam, Kazutoshi Wakabayashi*

The papers of this session tackle various important problems for modern high level synthesis systems. The first paper proposed a new list scheduling method using genetic algorithms for a heterogeneous multiprocessor system. The second paper takes advantage of novel bit-level chaining and non-integer multiple-cycling. The third paper provides a data-flow scheduling model based on a bounded set of protocol-defined resources. The last paper presents an efficient code motion technique across basic blocks.

17.1 Genetic List Scheduling Algorithm for Scheduling and Allocation on a Loosely Coupled Heterogeneous Multiprocessor System

Martin Grajcar - Univ. of Passau, Passau, Germany

17.2 Performance-Driven Scheduling With Bit-Level Chaining

Sanghun Park - LG Semicon Co. Ltd, Seoul, Korea
Kiyoung Choi - Seoul National Univ., Seoul, Korea

17.3SA Model for Scheduling Protocol-Constrained Components and Environments

Steve Haynal, Forrest D. Brewer - Univ. of California, Santa Barbara, CA

17.4SA Reordering Technique for Efficient Code Motion

Luiz C. V. Dos Santos, Jochen A.G. Jess - Eindhoven Univ. of Technology, Eindhoven, The Netherlands



SESSION 18

ROOM: AUDITORIUM A

SYMBOLIC MODEL CHECKING

Chair: *Andreas Kuehlmann* - Univ. of California, Berkeley, CA

Organizers: *Andreas Kuehlmann, Kunle Olukotun*

This session covers three distinct areas in symbolic model checking. The first paper presents a novel technique to analyze the coverage of properties verified by model checking. The next two papers cover new improvements on symbolic reachability analysis. The last paper presents the application of a SAT solver to model checking.

§18.1 Coverage Estimation for Symbolic Model Checking

Yatin V. Hoskote, *Timothy Y. Kam* - Intel Corp., Hillsboro, OR

Pei-Hsin Ho - Synopsys, Inc., Beaverton, OR
Xudong Zhao - Intel Corp., Hillsboro, OR

18.2 Improving Symbolic Traversals by Means of Activity Profiles

Gianpiero Cabodi, *Paolo E. Camurati, Stefano Quer* - Politecnico di Torino, Torino, Italy

18.3S Improved Approximate Reachability Using Auxiliary State Variables

Shankar G. Govindaraju, *David L. Dill, Jules P. Bergmann* - Stanford Univ., Stanford, CA

18.4S Symbolic Model Checking Using Sat Procedures Instead of BDDs

Armin Biere - Carnegie Mellon Univ., Pittsburgh, PA

Alessandro Cimatti - Institute for Scientific Research, Povo, Italy

Edmund M. Clarke - Carnegie Mellon Univ., Pittsburgh, PA

Masahiro Fujita - Fujitsu Labs. of America, Inc., Sunnyvale, CA

Yunshan Zhu - Carnegie Mellon Univ., Pittsburgh, PA

SESSION 19

ROOM: AUDITORIUM C

DSP DESIGN TECHNIQUES AND IMPLEMENTATIONS

Chair: *Jan M. Rabaey* - Univ. of California, Berkeley, CA

Organizers: *David Blaauw, Neil Weste*

Digital signal processing continues to be a growing market for VLSI design. In this session, two papers are presented on design exploration for media processors and multimedia systems. The last two papers present successful university implementations of DSP designs.

19.1 Power Efficient Mediaprocessors: Design Space Exploration

Johnson Kin, Chunho Lee, William H. Mangione-Smith, Miodrag Potkonjak - Univ. of California, Los Angeles, CA

19.2 Global Multimedia System Design Exploration Using Accurate Memory Organization Feedback

Arnout Vandecappelle, *Miguel Miranda, Erik Brockmeyer, Francky Catthoor, Diederik Verkest* - IMEC, Leuven, Belgium

19.3S DESIGN CONTEST FINALIST: Implementation of a Scalable MPEG-4 Wavelet-Based Visual Texture Compression System

Lode Nachtergaele, *Bart Vanhoof, Mercedes Peón, Gauthier Lafruit, Jan Bormans, Ivo Bolsens* - IMEC, Leuven, Belgium

19.4S DESIGN CONTEST FINALIST: A 10 MBIT/s Upstream Cable Modem with Automatic Equalization

Patrick R. Schaumont, *Radim Cmar, Serge Vernalde, Marc Engels* - IMEC, Leuven, Belgium

SESSION 20

ROOM: AUDITORIUM B

PANEL: CELL LIBRARIES - BUILD VS. BUY, STATIC VS. DYNAMIC

Chair: *Kurt Keutzer* - Univ. of California, Berkeley, CA

Organizer: *Emil Girczyc*

Cell libraries now determine the density, performance, and power of cell based circuit designs. Traditionally, designers used the cell libraries provided by their silicon source (internal division or ASIC vendor). However, recent changes in technology and business practices make several cell library choices available to design groups: silicon vendors, third party library vendors, internally created, and dynamic cell creation. This panel describes the variety of cell library choices and debates when designers should use each available source of cell libraries.

PANEL MEMBERS:

Jeffrey L. Burns - IBM, Corp., Austin, TX
Martin Lefebvre - Cadabra Design

Technology, Inc., Santa Clara, CA
Jeff Lewis - Artisan Components, Inc. Sunnyvale, CA

Jay Maxey - Texas Instruments, Dallas, TX

David Pietromonaco - Hewlett-Packard Co., Palo Alto, CA

Kurt A. Wolf - TSMC, San Jose, CA



10:30
to
12:00

SESSION 21

ROOM: 291

PARTITIONING AND LINEAR PLACEMENT

Chair: *Chung-Kuan Cheng* - Univ. of California at San Diego, La Jolla, CA

Organizers: *Sharad Malik; Andrew B. Kahng and Malgorzata Marek-Sadowska*

This session begins with a description of WMETIS 1.5, the latest advance in k-way netlist partitioning. Next, two short papers respectively point out the need for detailed, principled reporting methodology in the partitioning community, and also point out the qualitative change in difficulty when vertices are fixed. The session concludes with a general framework for amplifying local search and its successful application to linear placement.

21.1 Multilevel K-WAY Hypergraph Partitioning

George Karypis, *Vipin Kumar* - Univ. of Minnesota, Minneapolis, MN

21.2S Hypergraph Partitioning for VLSI CAD: Methodology for Reporting, and New Results

Andrew Caldwell, *Andrew B. Kahng* - Univ. of California, Los Angeles, CA

Andrew Kennings - Ryerson Polytechnic Univ., Toronto, Canada

Igor L. Markov - Univ. of California, Los Angeles, CA

21.3S Hypergraph Partitioning with Fixed Vertices

Andrew Caldwell, *Andrew B. Kahng*, **Igor L. Markov** - Univ. of California, Los Angeles, CA

21.4 Relaxation and Clustering in a Local Search Framework: Application to Linear Placement

Sung-Woo Hur, *John Lillis* - Univ. of Illinois at Chicago, Chicago, IL

SESSION 22

ROOM: 293

TECHNOLOGY DEPENDENT SYNTHESIS AND OPTIMIZATION

Chair: *Massoud Pedram* - Univ. of Southern California, Los Angeles, CA

Organizers: *Malgorzata Marek-Sadowska, Jason Cong*

This session presents three papers which bring technology level details into the synthesis and optimization process. The first paper proposes an approach for storing compactly the costs and arrival time data at a node in the subject graph. The second paper describes algorithms for mapping to FPGAs with non-uniform pin delays and fast interconnections. The third paper presents an algorithm for minimizing power consumption in domino circuits by output phase assignment.

22.1 An Alpha-Approximate Algorithm for Delay-Constrained Technology Mapping

Sumit Roy, *Krishna P. Belkhale* - Cadence Design Systems, Inc., Santa Clara, CA
Prithviraj Banerjee - Northwestern Univ., Evanston, IL

22.2 Technology Mapping for FPGAs with Nonuniform Pin Delays and Fast Interconnections

Jason Cong, *Yean-Yow Hwang*, **Songjie Xu** - Univ. of California, Los Angeles, CA

22.3 Automated Phase Assignment for the Synthesis of Low Power Domino Circuits

Priyadarsan Patra - Intel Corp., Hillsboro, OR
Unni K. Narayanan - Intel Corp., Santa Clara, CA



SESSION 23

ROOM: AUDITORIUM A

ADVANCES IN SYMBOLIC SIMULATION

Chair: *David L. Dill* - Stanford Univ., Stanford, CA

Organizers: *Kunle Olukotun, Andreas Kuehlmann*

The papers in this session tackle the important problem of extending symbolic simulation to handle large designs. The first paper uses test techniques, the second paper combines symbolic simulation with logic simulation, the third paper introduces a new logic for verifying pipelined processors and the fourth paper suggests an alternative method for dealing with input constraints.

23.1 Enhancing Simulation With BDDs and ATPG

Malay Ganai, Adnan Aziz - Univ. of Texas, Austin, TX

Andreas Kuehlmann - Univ. of California, Berkeley, CA

23.2 Cycle-Based Symbolic Simulation of Gate-Level Synchronous Circuits

Maurizio Damiani - C2 Design Automation, Santa Clara, CA

Valeria M. Bertacco - Synopsys, Inc., Mountain View, CA

Stefano Quer - Politecnico di Torino, Torino, Italy

23.3S Exploiting Positive Equality and Partial Non-Consistency in the Formal Verification of Pipelined Microprocessors

Miroslav N. Velev, Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

23.4S Formal Verification Using Parametric Representations of Boolean Constraints

Mark D. Aagaard, Robert Jones, Carl-Johan H. Seger - Intel Corp., Hillsboro, OR

SESSION 24

ROOM: AUDITORIUM C

SYSTEM LEVEL DESIGN METHODOLOGY AND CASE STUDIES

Chair: *Ivo Bolsens* - IMEC, Leuven, Belgium

Organizers: *Asawaree Kalavade, Kenji Yoshida*

This session focuses on practical methodologies for system-level design. The first paper describes a DSP benchmark that is applicable to system level testing. The second paper describes a visualization based interactive framework for hardware/software partitioning. The last two papers describe case studies on the design for large scale systems.

24.1 Vertical Benchmarks for CAD

Chris Inacio, Herman Schmit, David Nagle, Andrew Ryan, Ying-Fai Tong, Donald E. Thomas, Beu Klass - Carnegie Mellon Univ., Pittsburgh, PA

24.2 A Framework for User Assisted Design Space Exploration

Xiaobo (Sharon) Hu - Univ. of Notre Dame, Notre Dame, IN

Garrison Greenwood, Sai Ravichandran - Western Michigan Univ., Kalamazoo, MI
Gang Quan - Univ. of Notre Dame, Notre Dame, IN

24.3S Fast Prototyping: A System Design Flow Applied to a Complex System-on-Chip Multiprocessor Design

Richard Hersemeule, Benoit Clement, Pierre Coulomb, Francois Pogodalla - STMicroelectronics, Meylan, France
Etienne Lantreibeq - STMicroelectronics, Crolles Cedex, France

Bernard Ramanadin - STMicroelectronics, San Jose, CA

24.4S Verification and Management of a Multimillion-Gate Embedded Core Design

Johann Notbauer, Thomas W. Albrecht, Georg Niedrist, Stefan Rohringer - Siemens AG, Vienna, Austria

SESSION 25

ROOM: AUDITORIUM B

PANEL: PARASITIC EXTRACTION ACCURACY: HOW MUCH IS ENOUGH?

Chair: *Paul Franzon* - North Carolina State Univ., Raleigh, NC

Organizers: *Mark Basel, Paul Franzon*

A recent article in EE Times forecast that future IC yields will fall dramatically as on-chip noise and timing issues become paramount. Interconnect parasitics — capacitance, resistance and inductance — will be the main source of these timing and noise problems. The purpose of this panel is to address the tradeoffs between different approaches to achieving sufficient extraction accuracy with reasonable run times. Should the priority be given to fast, very accurate extraction, or is a 'flow' better, whereby higher level information is used to filter nets before extraction? Alternatively, do sensible 'design rules' reduce the need for interconnect extraction? How are advanced needs, such as handling process variation and inductance, best addressed? What does the term 'extraction accuracy' even mean when evaluating the alternative approaches?

PANEL MEMBERS:

Mark Basel - Cadence Design Systems, Inc., Cary, NC

Paul Franzon - North Carolina State Univ., Raleigh, NC

Aki Fujimura - Simplex Solutions, Inc. Sunnyvale, CA

Sharad Mehrotra - IBM Corp., Austin, TX

Ron Preston - Compaq Computer Corp., Shrewsbury, MA

Robin Sarma - Texas Instruments, Dallas, TX

Marty Walker - Frequency Technology, Inc., San Jose, CA



2:00
to
4:00

§ - denotes best paper

SESSION 26

ROOM: 291

CIRCUIT OPTIMIZATION FOR POWER AND PERFORMANCE

Chair: Andrew B. Kahng - Univ. of California, Los Angeles, CA

Organizers: Andrew B. Kahng, Hidetoshi Onodera

This session begins with three papers that detail use of multi-threshold CMOS, circuit design innovations, and circuit sizing techniques to achieve new methodologies for leakage power minimization. The fourth paper gives a technique for glitch power reduction. The session concludes with a description of Einstuner, a circuit optimizer that integrates dynamic simulation and nonlinear optimization within a static-timing framework.

26.1 Mixed- V_{th} (MVT) CMOS Circuit Design Methodology for Low Power Applications

Liqiong Wei, Zhanping Chen, Kaushik Roy - Purdue Univ., West Lafayette, IN
Yibin Ye, Vivek De - Intel Corp., Hillsboro, OR

26.2 Stand-By Power Minimization Through Simultaneous Threshold Voltage Selection and Circuit Sizing

Tim Edwards, Supamas Sirichotiyakul, Chanhee Oh, Jingyan Zuo - Motorola, Inc., Austin, TX
Abhijit Dharchoudhury - Intel Corp., Austin, TX
Rajendran V. Panda, **David Blaauw** - Motorola, Inc., Austin, TX

26.3§ Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS

Mark C. Johnson - Rose-Hulman Institute of Technology, Terre Haute, IN
Dinesh Somasekhar, Kaushik Roy - Purdue Univ., West Lafayette, IN

26.4§A Practical Gate Resizing Technique Considering Glitch Reduction for Low Power Design

Masanori Hashimoto, Hidetoshi Onodera, Keikichi Tamaru - Kyoto Univ., Kyoto, Japan

26.5 Gradient-Based Optimization of Custom Circuits Using A Static-Timing Formulation

Andrew R. Conn, Ibrahim M. Elfadel, Walter W. Molzen, Jr. - IBM Corp., Yorktown Heights, NY
Peter R. O'Brien - IBM Corp., Austin, TX
Philip N. Strenski, **Chandu Visweswariah**, Chagam B. Whan - IBM Corp., Yorktown Heights, NY

SESSION 27

ROOM: 293

INTERACTION OF SYNTHESIS AND LAYOUT

Chair: Lukas Van Ginneken - Magma Design Automation, Inc., Cupertino, CA

Organizers: Jason Cong, Malgorzata Marek-Sadowska

The papers in this session explore the linkage and interaction between synthesis and layout. The first paper combines circuit partitioning and clustering with retiming for performance optimization. The second paper proposes a new decision diagram structure that enables wave pipelining with predictable layout delay. The last two papers consider interconnect modeling and optimization during buffer insertion.

27.1 Simultaneous Circuit Partitioning/Clustering with Retiming for Performance Optimization

Jason Cong, Honching Li, **Chang Wu** - Univ. of California, Los Angeles, CA

27.2 Wave Pipelining in Yadd: A Novel Non-Iterative Synthesis and Layout Technique

Arindam Mukherjee - Univ. of California, Santa Barbara, CA
Ranganathan Sudhakar - Stanford Univ., Stanford, CA
Malgorzata Marek-Sadowska, Stephen I. Long - Univ. of California, Santa Barbara, CA

27.3 Merlin: Semi-Order-Independent Hierarchical Buffered Routing Tree Generation Using Local Neighborhood Search

Amir H. Salek, Jinan Lou, Massoud Pedram - Univ. of Southern California, Los Angeles, CA

27.4 Buffer Insertion with Accurate Gate and Interconnect Delay Computation

Charles J. Alpert, Anirudh Devgan, Stephen T. Quay - IBM Corp., Austin, TX



SESSION 28

ROOM: AUDITORIUM A

INTERCONNECT ISSUES FOR DEEP-SUBMICRON DESIGN

Chair: *Mojib C. Chian* - Rockwell Semiconductor Systems, Newport Beach, CA

Organizers: *Anantha Chandrakasan, Tadahiro Kuroda*

Deep-Submicron designs pose new challenges for interconnect parasitic estimation and optimization. The first paper describes a control signal ordering scheme to minimize the switching wire delay and power consumption. The second paper presents a methodology for power and ground network pre-layout for low net resistance and better parasitic predictability. The third paper introduces a procedure to predict wire delay in bi-directional buses and driver sizing. The last two papers present interconnect optimization through repeater insertion and estimation models for optimal wire sizing.

§28.1 Reducing Cross-Coupling Among Interconnect Wires in Deep-Submicron Datapath Design

Joon-Seo Yim - Lg Cit, Seoul, Korea

Chong-Min Kyung - Kaist, Taejeon, Korea

28.2 A Novel VLSI Layout Fabric for Deep Sub-Micron Applications

Sunil P. Khatri, Amit Mehrotra, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

Ralph H.J.M. Otten - Delft Univ. of Technology, Delft, The Netherlands

28.3 Improved Delay Prediction for On-Chip Buses

Real Pomerleau, Paul Franzone, Griff L. Bilbro - North Carolina State Univ., Raleigh, NC

28.4S Noise-Aware Repeater Insertion and Wire Sizing for On-Chip Interconnect Using Hierarchical Moment-Matching

Chung-Ping Chen, Noel Menezes - Intel Corp., Hillsboro, OR

28.5S Interconnect Estimation and Planning for Deep Submicron Designs

Jason Cong, David Zhigang Pan - Univ. of California, Los Angeles, CA

SESSION 29

ROOM: AUDITORIUM C

DESIGN ENTRY AND SPECIFICATION

Chair: *Asawaree Kalavade* - Bell Labs., Lucent Technologies, Murray Hill, NJ

Organizers: *Kenji Yoshida, Ivo Bolsens*

This session focuses on system-level specification techniques. The first paper describes a specification language that combines C and Esterel. The next paper describes a model for representation of functional variants, i.e., systems with reconfigurable components. The third paper describes a Verilog-based specification framework. The final paper describes a constraint management methodology.

29.1 ECL: A Specification Environment for System-Level Design

Ellen M. Sentovich - Cadence Berkeley Labs., Berkeley, CA

Luciano Lavagno - Politecnico di Torino, Torino, Italy

29.2 Representation of Function Variants for Embedded System Optimization and Synthesis

Kai Richter, Dirk Ziegenbein, Rolf Ernst - Technical Univ. of Braunschweig, Braunschweig, Germany

Lothar Thiele - Swiss Federal Institute of Technology, Zurich, Switzerland

Juergen Teich - Univ. Gh Paderborn, Paderborn, Germany

29.3 Vex - A Cad Toolbox

Jules P. Bergmann, Mark A. Horowitz - Stanford Univ., Stanford, CA

29.4 Constraint Management for Collaborative Electronic Design

Juan Antonio Carballo, Stephen W. Director - Univ. of Michigan, Ann Arbor, MI

SESSION 30

ROOM: AUDITORIUM B

PANEL: MEMS CAD: BEYOND MULTI-MILLION TRANSISTORS

Chair: *Kristopher Pister* - Univ. of California, Berkeley, CA

Organizers: *Takahide Inoue, Kristopher Pister*

Existing MEMS products boast more than a million electrical and mechanical components on a single chip. MEMS fabrication technology has leveraged decades of IC expertise. MEMS CAD tools now beginning to leverage corresponding decades of IC CAD expertise to address the exciting and unique electro-mechanical co-design problems from the physical through system level design.

A tutorial introduction will be provided by Dr. Al Pisano, director of the DARPA MEMS program, followed by a panel discussion by MEMS CAD tool developers and tool users from industry.

PANEL MEMBERS:

Gary K. Fedder - Carnegie Mellon Univ., Pittsburgh, PA

John R. Gilbert - Microcosm

Technologies, Inc., Cambridge, MA

Mike Horton - CrossBow Technologies, Inc., San Jose, CA

Al Pisano - DARPA/ETO, Arlington, VA

John Rynchik - Visteon Technical Ctr., Dearborn, MI

Nicholas R. Swart - Analog Devices Inc., Cambridge, MA



4:30
to
6:00

SESSION 31

ROOM: 291

EXTRACTION OF CAPACITANCE AND SUBSTRATE MODELS

Chair: *David D. Ling* - IBM Corp., Yorktown Heights, NY

Organizers: *Joel R. Phillips, Louis Scheffer*

This session features advances in methods for extraction of circuit interconnect and substrate models. The first paper presents a new multiscale transformation method for accelerating integral-equation based capacitance extractors. Efficiently incorporating non-uniform meshes into integral equation solvers is the topic of the second paper. The third paper presents techniques for accurate extraction and modeling of substrate resistance meshes.

31.1 A Multiscale Method for Fast Capacitance Extraction

Johannes Tausch - Southern Methodist Univ., Dallas, TX

Jacob K. White - Massachusetts Institute of Technology, Cambridge, MA

31.2 Efficient Capacitance Computation for Structures with Non-Uniform Adaptive Surface Meshes

Vikram Jandhyala, Scott Savage, Eric Bracken, Zoltan Cendes - Ansoft Corp., Pittsburgh, PA

31.3 Substrate Modeling and Lumped Substrate Resistance Extraction for CMOS ESD/Latchup Circuit Simulation

Tong Li, Ching-Han Tsai, Elyse Rosenbaum, Sung-Mo Kang - Univ. of Illinois, Urbana, IL

SESSION 32

ROOM: 293

HIGH-LEVEL TECHNIQUES FOR LOW POWER

Chair: *Sunil D. Sherlekar* - Silicon Automation Systems, Bangalore, India

Organizers: *Sunil D. Sherlekar, Farid Najm*

This session deals with high-level design, synthesis and simulation techniques for low power. The first paper proposes a technique for system-level dynamic power management. The second paper proposes a parallel simulation technique for power simulation. Finally, the last short paper describes a behavioral synthesis technique for low power using multiple precision arithmetic.

32.1 Dynamic Power Management Based on Continuous Time Markov Decision Process

Qinru Qiu, Qing Wu, Massoud Pedram - Univ. of Southern California, Los Angeles, CA

32.2 Parallel Mixed-Level Power Simulation Based on Spatio-Temporal Circuit Partitioning

Mauro Chinosi - SGS-Thomson Microelectronics, Agrate Brianza, Italy

Roberto Zafalon - STMicroelectronics, Agrate Brianza, Italy

Carlo Guardiani - SGS-Thompson Microelectronics, Agrate Brianza, Italy

32.3S Low-Power Behavioral Synthesis Optimization Using Multiple Precision Arithmetic

Milos Ercegovac, Darko Kirovski, Miodrag Potkonjak - Univ. of California, Los Angeles, CA

SESSION 33

ROOM: AUDITORIUM A



SYSTEM-LEVEL VERIFICATION AND TEST

Chair: Kenji Yoshida - Toshiba Corp., Kawasaki, Japan

Organizers: Asawaree Kalavade, Ivo Bolsens

Verification and test are big problems in developing complex systems on chip. The first two papers of this session address system level verification methodologies and the third paper talks about test methodologies for core-based systems on chip.

33.1 A Methodology for the Verification of a System on Chip

Daniel Geist, Giora Biran, Tamara Arons, Yvgeny Nustov, Michael Slavkin, Monica Farkash, Karen Holtz, Andy Long, Dave King, Steve Barret- IBM Haifa Research Lab., Haifa, Israel

33.2 Iceberg: An Embedded In-Circuit Emulator Synthesizer for Microcontrollers

Ing-Jer Huang, Tai-An Lu - National Sun Yat-Sen Univ., Kaohsiung, Taiwan ROC

33.3 Microprocessor Based Testing for Core-Based System on Chip

Christos A. Papachristou, Francis Martin, Mehrdad Nourani - Case Western Reserve Univ., Cleveland, OH

SESSION 34

ROOM: AUDITORIUM C

LOGIC AND HIGH-LEVEL SYNTHESIS METHODOLOGIES

Chair: Mahadevamurty Nemani - Intel Corp., Santa Clara, CA

Organizers: Randolph E. Harr, Telle Whitney

The papers in this session address some emerging methodologies in logic and high-level synthesis. The first paper presents a netlist partitioning scheme for better timing convergence in deep-submicron designs. The second paper reports on the experiences and lessons learned from using two design flows (RTL and behavioral synthesis) for a real design. The final paper presents a technique for integrating engineering change within behavioral synthesis.

34.1 Using Partitioning to Help Convergence in the Standard-Cell Design Automation Methodology

Hema Kapadia, Mark A. Horowitz - Stanford Univ., Stanford, CA

34.2 Comparing RTL and Behavioral Design Methodologies in the Case of a 2M Transistors ATM Shaper

Moussa Imed, Sugar Zoltan, Suescun Rodolph - TIMA-CMP, Grenoble, France
Diaz Nava Mario - STMicroelectronics, Crolles, France
Pavessi Marco, Crudo Salvatore, Gazi Luca - Italtel, Settimo Milanese, Italy
Jerraya Ahmed Amine - TIMA-CMP, Grenoble, France

34.3 Engineering Change: Methodology and Applications to Behavioral and System Synthesis

Darko Kirovski, Miodrag Potkonjak - Univ. of California, Los Angeles, CA

SESSION 35

ROOM: AUDITORIUM B
RECONFIGURABLE

SYSTEMS

Chair: Telle Whitney - Malleable Microsystems, Mountain View, CA

Organizers: Vivek Tiwari, Randolph E. Harr

Dynamic reconfigurable computing is an emerging area with a unique set of DA opportunities. This session begins with an embedded tutorial overview of the area, and then presents a partitioning approach and novel architecture that exploit the dynamic characteristics of these reconfigurable systems.

35.1 EMBEDDED TUTORIAL: Reconfigurable Computing; What, Why, and Implications for Design Automation

Andre Dehon, John Wawrzynek - Univ. of California, Berkeley, CA

35.2 An Automated Temporal Partitioning and Loop Fission Approach for FPGA Based Reconfigurable Synthesis of DSP Applications

Meenakshi Kaul, Ranga Vemuri, Sriram Govindarajan, Iyad E. Ouass - Univ. of Cincinnati, Cincinnati, OH

35.3 Dynamically Reconfigurable Architecture for Image Processor Applications

Alexandro Magno S. Adario, Eduardo L. Roehle, **Sergio Bampi** - UFRGS, Porto Alegre, Brazil

SESSION 36

ROOM: 291

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Thursday, June 24

technical
program

Thursday
Keynote
Address
1:00 to 1:45
AUDITORIUM B

no badge
required to
attend the
Thursday
Keynote

8:30
to
10:00

RF SIMULATION

Chair: *L. Miguel Silveira* - Technical Univ. of Lisbon, Lisbon, Portugal

Organizers: *Alan Mantooth, Hidetoshi Onodera*

In this session there are three papers that report on advancements that pertain to RF simulation. The first utilizes an extension to MPDE which involves time warping to capture complex dynamics in autonomous nonlinear systems. This paper presents the approach for analyzing forced and unforced oscillatory systems. The second paper describes advances in multi-frequency time algorithms that enable application to large circuits. The final paper presents a fast Krylov-subspace spectral method that overcomes the reduced efficiency of standard harmonic balance in the case of rapid transitions.

36.1 Multi-Time Simulation of Voltage-Controlled Oscillators

Onuttom Narayan - Univ. of California, Santa Cruz, CA
Jaijeet S. Roychowdhury - Bell Labs., Lucent Technologies, Murray Hill, NJ

36.2 Efficient Computation of Quasi-Periodic Circuit Operating Conditions Via a Mixed Frequency/Time Approach

Dan Feng, *Joel R. Phillips, Keith Nabors, Kenneth S. Kundert* - Cadence Design Systems, Inc., San Jose, CA
Jacob K. White - Massachusetts Institute of Technology, Cambridge, MA

36.3 Time-Mapped Harmonic Balance

Ognen J. Nastov - Motorola, Inc., Austin, TX
Jacob K. White - Massachusetts Institute of Technology, Cambridge, MA

SESSION 37

ROOM: 293

ADVANCED TEST GENERATION AND DIAGNOSIS

Chair: *Janusz Rajski* - Mentor Graphics Corp., Wilsonville, OR

Organizers: *Yervant Zorian, Janusz Rajski*

This session presents an advanced set of techniques used for test generation and diagnosis. The first paper introduces a technique to handle testing of gigahertz processors; the second introduces a novel test generation technique using compaction and an iterative process. Finally the third paper provides a new diagnosis techniques for multiple errors.

37.1 Test Generation for Gigahertz Processors Using an Automatic Functional Constraint Extractor

Raghuram Tupuri - AMD, Austin, TX
Arun Krishnamachary, Jacob A. Abraham - Univ. of Texas, Austin, TX

37.2 Proptest: A Property Based Test Pattern Generator for Sequential Circuits Using Test Compaction

Ruifeng Guo, Sudhakar M. Reddy, Irith Pomeranz - Univ. of Iowa, Iowa City, IA

37.3 Multiple Error Diagnosis Based on Xlists

Vamsi Boppana, *Rajarshi Mukherjee, Jawahar Jain, Masahiro Fujita* - Fujitsu Labs. of America, Inc., Sunnyvale, CA
Pradeep Bollineni - Iowa State Univ., Ames, IA

SESSION 38

ROOM: AUDITORIUM A

Please be advised that the two Keynotes and some of the Technical Sessions will be video taped during the conference.



RTL CIRCUIT SIMULATION

Chair: *Luciano Lavagno* - Politecnico di Torino, Torino, Italy

Organizers: *Neil Weste, Teresa Meng*

Verification of RTL circuits remains a bottleneck in design verification. In this session, methods are presented for RTL vector generation, two state simulation techniques, and for extracting timing information.

38.1 Simulation Vector Generation from HDL Descriptions for Observability Enhanced-Statement Coverage

Farzan Fallah - Fujitsu Labs. of America, Sunnyvale, CA

Pranav Ashar - NEC USA, C&C Research Labs., Princeton, NJ

Srinivas Devadas - Massachusetts Institute of Technology, Cambridge, MA

38.2 A Two-State Methodology for RTL Logic Simulation

Lionel Bening - Hewlett-Packard Co., Richardson, TX

38.3 An Approach for Extracting RT Timing Information to Annotate Algorithmic VHDL Specifications

Cordula Hansen - FZI, Karlsruhe, Germany

Francisco Nascimento - Univ. of Tuebingen, Tuebingen, Germany

Wolfgang Rosenstiel - FZI/Univ. of Tuebingen, Tuebingen, Germany

SESSION 39

ROOM: AUDITORIUM C

CAD SOLUTIONS USING FPGAs

Chair: *Rajesh K. Gupta* - Univ. of California, Irvine, CA

Organizers: *Telle Whitney, Vivek Tiwari*

Reconfigurable logic can be used to build high performance computational platforms to solve interesting CAD-theoretic problems. Papers in this session show how FPGA-based systems can be applied to solve satisfiability, fault diagnosis and compilation problems.

39.1 A Massively-Parallel Easily-Scalable Satisfiability Solver Using Reconfigurable Hardware

Miron Abramovici, José T. de Sousa - Bell Labs., Lucent Technologies, Murray Hill, NJ

Daniel G. Saab - Case Western Reserve Univ., Cleveland, OH

39.2 Dynamic Fault Diagnosis on Reconfigurable Hardware

Fatih Kocan, Daniel G. Saab - Case Western Reserve Univ., Cleveland, OH

39.3 Hardware Compilation for FPGA-Based Configurable Computing Machines

Xiaohan Zhu, Bill Lin - Univ. of California at San Diego, La Jolla, CA

SESSION 40

ROOM: AUDITORIUM B

TECHNOLOGY DIRECTIONS

Chair: *Bryan D. Ackland* - Bell Labs., Lucent Technologies, Holmdel, NJ

Organizer: *Bryan D. Ackland*

The required capabilities of our design tools and methodologies are heavily influenced by the physical and electrical characteristics of the underlying technology. In this session, we explore where our VLSI technologies are heading. In the first paper we take a look at conventional CMOS at 0.18 μ and beyond - including copper and local interconnect and low-K dielectrics. In the second we examine the impact that SOI technologies will have on our circuit designs and CAD tool environment.

40.1 INVITED PAPER: 0.18 μ CMOS and Beyond

David Eaglesham - Bell Labs., Lucent Technologies, Murray Hill, NJ

40.2 INVITED PAPER: SOI Digital CMOS VLSI - A Design Perspective

Ching-Te Chuang, Ruchir Puri - IBM Corp., Yorktown Heights, NY

(45 minute presentations)

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Thursday, June 24

technical
program10:30
to
12:00§ - denotes
best paper**SESSION 41****ROOM:** 291**TIMING ANALYSIS AND OPTIMIZATION****Chair:** *Thomas G. Szymanski* - Bell Labs., Lucent Technologies, Murray Hill, NJ**Organizers:** *Kunle Olukotun, Sharad Malik*

This session covers recent advances in timing analysis and optimization. We begin by looking at the development of inductance models and their use in interconnect optimization. Next a variant of retiming is proposed as a timing optimization technique for deep-submicron technology. Finally, we look at false path issues in IP specification and practical microprocessor design.

41.1S Equivalent Elmore Delay for RLC Trees**Yehea I. Ismail, Eby G. Friedman** - Univ. of Rochester, Rochester, NY**José L. Neves** - IBM Microelectronics, East Fishkill, NY**41.2S** Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits**Yehea I. Ismail, Eby G. Friedman** - Univ. of Rochester, Rochester, NY**41.3** Retiming for DSM with Area-Delay Trade-Offs and Delay Constraints**Abdallah Tabbara, Robert K. Brayton, A. Richard Newton** - Univ. of California, Berkeley, CA**41.4S** Functional Timing Analysis for IP Characterization**Hakan Yalcin, Mohammad Mortazavi, Robert Palermo, Cyrus S. Bamji** - Cadence Design Systems, Inc., San Jose, CA**Karem Sakallah** - Univ. of Michigan, Ann Arbor, MI**41.5S** Detecting False Timing Paths: Experiments on PowerPC™ Microprocessors**Richard Raimi** - Motorola, Inc., Austin, TX
Jacob A. Abraham - Univ. of Texas, Austin, TX**SESSION 42****ROOM:** 293**BUILT-IN SELF-TEST SOLUTIONS****Chair:** *Yervant Zorian* - LogicVision, Inc., San Jose, CA**Organizers:** *Janusz Rajski, Yervant Zorian*

This session introduces new Built-In Self-Test Solutions from synthesizing data paths for self-testability, to increasing fault coverage of Scan-BIST by using multiple capture cycles, to on-chip test sequence generation for at-speed testing.

42.1 On ILP Formulations for Built-In Self-Testable Data Path Synthesis**Han Bin Kim, Dong S. Ha** - Virginia Polytechnic Institute, Blacksburg, VA**Takeshi Takahashi** - Advantest America R&D Ctr., Santa Clara, CA**42.2** Improving the Test Quality for Scan-Based BIST Using a General Test Application Scheme**Huan-Chih Tsai, Kwang-Ting (Tim) Cheng** - Univ. of California, Santa Barbara, CA**Sudipta Bhawmik** - Bell Labs., Lucent Technologies, Princeton, NJ**42.3** Built-In Test Sequence Generation for Synchronous Sequential Circuits Based on Loading and Expansion of Test Subsequences**Irith Pomeranz, Sudhakar M. Reddy** - Univ. of Iowa, Iowa City, IA



SESSION 43

ROOM: AUDITORIUM A

CLOCK, POWER DISTRIBUTION AND ANALOG ISSUES

Chair: *Abhijit Dharchoudhury* - Motorola, Inc., Austin, TX

Organizers: *Teresa Meng, David Blaauw*

Clock and power distribution are becoming increasingly difficult with process scaling and increased frequency. The first two papers in this session present new methods in clock and power distribution. The last paper presents testing methods for analog circuits.

43.1 Analysis of Performance Impact Caused by Power Supply Noise In Deep Submicron Devices

Yi-Min Jiang, Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara, CA

43.2 A Floorplan-Based Planning Methodology for Power and Clock Distribution in ASICs

Joon-Seo Yim, Seong-Ok Bae - Lg Cit, Seoul, Korea
Chong-Min Kyung - KAIST, Taejon, Korea

43.3 Digital Detection of Analog Parametric Faults

Ramesh Harjani, Bapiraju Vinnakota - Univ. of Minnesota, Minneapolis, MN

SESSION 44

ROOM: AUDITORIUM C

MODELING FOR DESIGN REUSE

Chair: *Han Yang* - Stanford Univ., Palo Alto, CA

Organizers: *Kenji Yoshida, David Ku*

This session discusses modeling technique to achieve design reuse. The first two papers focus on interface-based design using VHDL and object oriented modeling respectively. The other two papers describe the use of Java and Java beans for system modeling and reuse.

44.1 Application of High Level Interface-Based Design to Telecommunications System Hardware

Dyson Wilkes - Ericsson Components Ltd, Swindon, UK

M.M. Kamal Hashmi - International Computers Ltd., Manchester, UK

44.2 Hardware Reuse at the Behavioral Level

Patrick R. Schaumont, Radim Cmar, Serge Vernalde, Mark Engels, Ivo Bolsens - IMEC, Leuven, Belgium

44.3S Description and Simulation of Hardware/Software Systems with Java

Tommy Kuhn - Univ. Tuebingen, Tuebingen, Germany
Wolfgang Rosenstiel - FZI/Univ. of Tuebingen, Tuebingen, Germany
Udo Kebschull - Univ. of Leipzig, Leipzig, Germany

44.4S Java Driven Codesign and Prototyping of Networked Embedded Systems

Josef Fleischmann - Technical University of Munich, Munich, Germany
Klaus Buchenrieder, Rainer Kress - Siemens AG, Munich, Germany

SESSION 45

ROOM: AUDITORIUM B

PANEL: SUB-WAVELENGTH LITHOGRAPHY: HOW WILL IT IMPACT YOUR DESIGN FLOW?

Chair: *Andrew B. Kahng* - Univ. of California, Los Angeles, CA

Organizer: *Atul Sharan*

In the sub 0.25 micron regime, IC feature sizes become smaller than the wavelength of light used for mask exposure. Resultant light distortions create patterns on silicon that are substantially different from a GDSII layout. The techniques used to control these distortions have an impact on the design flow that may become as formidable as the recently addressed Deep Sub-Micron transition.

This session will address the design implications arising from techniques used to control sub-wavelength lithography. It will begin with an embedded tutorial on sub-wavelength mask design techniques and their resultant effect on the IC design process. The panel will then debate the extent of the resulting impact on IC performance, design flow, and CAD tools.

45.1 EMBEDDED TUTORIAL: Sub-Wavelength Lithography: How Will it Impact Your Design Flow

Y.C. "Buno" Pati - Numerical Technologies, Inc., Santa Clara, CA

PANEL MEMBERS:

Lance Glasser - KLA-Tencor Inc., San Jose, CA
Warren Groebman - Motorola Corp., Austin, TX
Andrew B. Kahng - Univ. of California, Los Angeles, CA
Robert Pack - Cadence Design Systems, Inc., San Jose, CA
Y. C. "Buno" Pati - Numerical Technologies, Inc., Santa Clara, CA
Kenneth V. Rousseau - Synopsys, Inc., Mountain View, CA
Atul Sharan - Numerical Technologies, Inc., Santa Clara, CA

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Thursday, June 24

technical
program2:00
to
4:00**SESSION 46****ROOM:** 291**SOFTWARE IMPLEMENTATION FOR DSP APPLICATIONS****Chair:** *Mahesh Mehendale* - Texas Instruments Ltd., Bangalore, India**Organizers:** *Sunil D. Sherlekar, Luciano Lavagno*

This session looks at software implementation issues of DSP from the system design to code generation level. The first paper deals with scheduling of concurrent specifications for multi-rate applications. The second paper deals with the important issue of memory size estimation for video applications. The next paper looks at optimization of code generation for irregular architectures. A short paper on performance analysis of DSP code follows. Finally, a short paper describes a software development environment for DSPs including scheduling, debugging and performance analysis.

46.1 Synthesis of Embedded Software Using Free-Choice Petri Nets*Marco Sgroi* - Univ. of California, Berkeley, CA
Luciano Lavagno - Cadence Design Systems, Inc., Berkeley, CA*Yosinori Watanabe* - Cadence Design Systems, Inc., Roma, Italy*Alberto L. Sangiovanni-Vincentelli* - Univ. of California, Berkeley, CA**46.2 Exact Memory Size Analysis in System Design: Handling Array Computations Without Loop Unrolling**
Ying Zhao, Sharad Malik - Princeton Univ., Princeton, NJ**46.3 Constraint Driven Code Selection for Fixed-Point DSPs****Steven Bashford, Rainer Leupers** - Univ. of Dortmund, Dortmund, Germany**46.4S Rapid Development of Optimized DSP Code from a High Level Description through Software Estimations****Alain Pegatoquet, Emmanuel Gresset** - VLSI Technology, Valbonne, France*Michel Auguin* - Univ. de Nice Sophia-Antipolis, Nice, France*Luc Bianco* - Laboratoire I3s, Nice, France**46.5S Software Environment for A Multiprocessor DSP****Asawaree Kalavade** - Bell Labs., Lucent Technologies, Murray Hill, NJ*Joe Othmer, Bryan D. Ackland, Kanwar J. Singh* - Bell Labs., Lucent Technologies, Holmdel, NJ**SESSION 47****ROOM:** 293**INTELLECTUAL PROPERTY PROTECTION USING WATERMARKING****Chair:** *Ken Hodor* - Actel Corp., Sunnyvale, CA**Organizers:** *Mike Murray, Neil Weste*

This session presents four different approaches for intellectual property protection using watermarking at different levels of the design process: FPGA layout, physical design, logic synthesis and behavioral level.

47.1 Robust FPGA Intellectual Property Protection through Multiple Small Watermarks**John Lach, William H. Mangione-Smith, Miodrag Potkonjak** - Univ. of California, Los Angeles, CA**47.2 Robust Techniques for Watermarking Sequential Circuit Designs****Arlindo L. Oliveira** - Cadence European Labs., Lisbon, Portugal**47.3 Effective Iterative Techniques for Fingerprinting Design IP***Andrew Caldwell, Hyun-Jin Choi, Andrew B. Kahng, Stefanus Mantik, Miodrag Potkonjak, Gang Qu, Jennifer L. Wong* - Univ. of California, Los Angeles, CA**47.4 Behavioral Synthesis Techniques for Intellectual Property Protection****Inki Hong, Miodrag Potkonjak** - Univ. of California, Los Angeles, CA



SESSION 48

ROOM: AUDITORIUM A

LOW POWER SYSTEM DESIGN TECHNIQUES

Chair: Vivek Tiwari - Intel Corp., Santa Clara, CA

Organizers: Tadahiro Kuroda, Mojoy Chian

System level techniques have significant impact on power dissipation. The first paper exploits dynamic voltage scaling and validates this idea for an encryption processor. The second paper presents an analysis of battery properties to enable new avenues for increasing battery life. The third paper presents a system level power estimation methodology and its use in design exploration. The final paper tackles clock power consumption through a globally asynchronous locally synchronous design style.

48.1 DESIGN CONTEST FINALIST: Design and Implementation of a Scalable Encryption Processor with Embedded Variable DC/DC Converter

James Goodman, Anantha Chandrakasan, Abram Darcy - Massachusetts Institute of Technology, Cambridge, MA

48.2 Design Considerations for Battery-Powered Electronics

Massoud Pedram, Qing Wu - Univ. of Southern California, Los Angeles, CA

48.3 Cycle-Accurate Simulation of Energy Consumption in Embedded Systems

Tajana Simunic, Luca Benini, Giovanni De Micheli - Stanford Univ., Stanford, CA

48.4 Lowering Power Consumption in Clock by Using Globally Asynchronous, Locally Synchronous Design Style

Ahmed Hemani, Thomas Meincke - KTH, Kista, Sweden

Shashi Kumar - Indian Institute of Technology, New Delhi, India

Adam Postula - Univ. of Queensland, Brisbane, Australia

Thomas Olsson, Peter Nilsson - Lund Univ., Lund, Sweden

Johnny Oberg, Peeter Ellervee - KTH, Kista, Sweden

Dan Lindkvist - Ericsson Radio Systems AB, Stockholm, Sweden

SESSION 49

ROOM: AUDITORIUM C

EMERGING DIRECTIONS

Chair: Randolph E. Harr - Synopsys, Inc., Mountain View, CA

Organizers: Anantha Chandrakasan, Mojoy Chian

Innovation is driven by dedicated people with a vision working in uncharted waters. This session covers three distinct problem areas, each of which will likely be a full session in the future.

49.1 A CAD Tool for Optical MEMS

Timothy P. Kurzweg, Steven P. Levitan - Univ. of Pittsburgh, Pittsburgh, PA

Philippe J. Marchand - Univ. of California at San Diego, La Jolla, CA

Jose A. Martinez, Kurt R. Prough, Donald M. Chiarulli - Univ. of Pittsburgh, Pittsburgh, PA

49.2 On Thermal Effects in Deep Sub-Micron VLSI Interconnects

Kaustav Banerjee, Amit Mehrotra, Alberto L. Sangiovanni-Vincentelli, Chenming Hu - Univ. of California, Berkeley, CA

49.3 Converting a 64b PowerPC Processor from CMOS Bulk to SOI Technology

David Allen, Derick Behrends - IBM Corp., Rochester, MN
Balsha R. Stanisic - IBM Corp., Rochester, MN

49.4 A Framework for Collaborative and Distributed Web-Based Design

Gangadhar Konduri, Anantha Chandrakasan - Massachusetts Institute of Technology, Cambridge, MA

SESSION 50

ROOM: AUDITORIUM B

INDUCTANCE ISSUES IN HIGH FREQUENCY DESIGN

Chair: David Blaauw - Motorola, Inc., Austin, TX

Organizers: Anantha Chandrakasan, David Blaauw

With process scaling and increased frequencies, the interconnect focus has shifted from RC to RLC models. This session presents a tutorial overview of parasitic inductance: estimation techniques, extraction, modeling, and design practices.

50.1 EMBEDDED TUTORIAL: Dealing with Inductance in High-Speed Chip Design

Phillip J. Restle, Albert E. Ruhli, Steven G. Walker - IBM Corp., Yorktown Heights, NY

50.2 INVITED PAPER: Interconnect Analysis: From 3-D Structures to Circuit Models

Jacob K. White - Massachusetts Institute of Technology, Cambridge, MA

50.3 INVITED PAPER: IC Analyses Including Extracted Inductance Models

Lawrence T. Pileggi, Michael Beattie - Carnegie Mellon Univ., Pittsburgh, PA

50.4 INVITED PAPER: On-Chip Inductance Issues in Multilayer, Multiconductor Systems

Shannon Morton - Compaq Computer Corp., Shrewsbury, MA

4:30
to
6:00**SESSION 51****ROOM:** 291**INSTRUCTION-LEVEL ASIP DESIGN****Chair:** *Sharad Malik* - Princeton Univ., Princeton, NJ**Organizers:** *Rajesh K. Gupta, David Ku*

Application Specific Instruction Set Processors (ASIPs) use customized instructions to achieve cost performance goals. Instruction set design is crucial to ASIP-based design. The first two papers in this session describe modeling and simulation methods for architecture. The last paper concerns design reuse for ASIP-based design.

51.1 A Methodology for Accurate Performance Evaluation in Architecture Exploration

George Hadjiyiannis, Pietro Russo, Srinivas Devadas - Massachusetts Institute of Technology, Cambridge, MA

51.2 LISA - Machine Description Language for Cycle-Accurate Models of Programmable DSP Architectures

Stefan Pees, Andreas Hoffmann - RWTH Aachen, Aachen, Germany
Vojin Zivojnovic - AXYS GmbH, Herzogenrath, Germany
Heinrich Meyr - RWTH Aachen, Aachen, Germany

51.3 Exploiting Intellectual Properties in ASIP Designs for Embedded DSP Software

Hoon Choi, Ju Hwan Yi, Jong-Yeol Lee, In-Cheol Park, Chong-Min Kyung - KAIST, Taejeon, Korea

SESSION 52**ROOM:** 293**ANALOG SYNTHESIS AND MODELING****Chair:** *Hidetoshi Onodera* - Kyoto Univ., Kyoto, Japan**Organizers:** *Alan Mantooth, Hidetoshi Onodera*

This session includes three papers for bringing analog synthesis and modeling into practice. The first paper discusses a simulation-based synthesis of custom analog cells running on a network of workstations. The second paper describes an approach for analog system synthesis from behavioral VHDL-AMS specifications. The third paper proposes a reduction technique for symbolic analysis utilizing a signal flow model of a circuit.

52.1 Maelstrom: Efficient Simulation-Based Synthesis of Custom Analog Cells

Michael Krasnicki, Rodney Phelps, Rob A. Rutenbar, L. Richard Carley - Carnegie Mellon Univ., Pittsburgh, PA

52.2 Behavioral Synthesis of Analog Systems Using Two-Layered Design Space Exploration

Alex Doboli, Adrian Nunez-Aldana, Nagu R. Dhanwada, Sreelakshmi Ganesan, Ranga Vemuri - Univ. of Cincinnati, Cincinnati, OH

52.3 Circuit Complexity Reduction for Symbolic Analysis of Analog Integrated Circuits

Walter Daems, Georges Gielen, Willy Sansen - Katholieke Univ. Leuven, Heverlee, Belgium



SESSION 53

ROOM: AUDITORIUM A

SIMULATION AND TEST

Chair: Miodrag Potkonjak - Univ. of California, Los Angeles, CA

Organizers: Mike Murray, Miodrag Potkonjak

This session presents two papers on the state-of-the-art industrial use of simulation in an innovative way. The last paper shows how a powerful new test technique is applied to a real-life design.

53.1 Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification

Lisa Marie Guerra - Conexant Systems, Inc., Newport Beach, CA

Joachim Fitzner - AXYS GmbH, Herzogenrath, Germany

Dipankar Talukdar - Conexant Systems, Inc., Newport Beach, CA

Chris Schlager - AXYS GmbH, Herzogenrath, Germany

Bassam Tabbara - Univ. of California, Berkeley, CA

Vojin Zivojnovic - AXYS GmbH, Herzogenrath, Germany

53.2 A Study in Coverage-Driven Test Generation

Mike Benjamin - STMicroelectronics, Bristol, UK

Daniel Geist, Alan Hartman, Yaron Wolfsthal - IBM Science and Technology, Haifa, Israel

Gerard Mas, Ralph Smeets - STMicroelectronics, Meylan, France

53.3 IC Test Using the Energy Consumption Ratio

Wanli Jiang, Bapiraju Vinnakota - Univ. of Minnesota, Minneapolis, MN

SESSION 54

ROOM: AUDITORIUM C

DESIGNING ON-CHIP INDUCTORS

Chair: Teresa Meng - Stanford Univ., Stanford, CA

Organizers: Teresa Meng, David Blaauw

Creating high quality on-chip inductors is a key enabler to highly integrated low cost, RF systems. In this session, two invited papers describe the current state-of-the-art in on-chip inductor design. The last paper presents a new approach to automatic optimization of on-chip inductors.

54.1 INVITED PAPER: Design Strategy of On-Chip Inductors for Highly Integrated RF Systems

Patrick Yue - T-Span Systems, Corp., Palo Alto, CA

Simon Wong - Stanford Univ., Stanford, CA

54.2 INVITED PAPER: The Simulation and Design of Integrated Inductors

Nathan Belk - Bell Labs., Lucent Technologies, Holmdel, NJ

Michel R. Frei, Ming-Ju Tsai, Andrew J. Becker, Kathleen L. Tokuda - Bell Labs., Lucent Technologies, Murray Hill, NJ

54.3S Optimization of Inductor Circuits Via Geometric Programming

Maria Del Mar Hershenson, Mohan Sunderarajan, Stephen Boyd, Thomas Lee - Stanford Univ., Stanford, CA

SESSION 55

ROOM: AUDITORIUM B

PANEL: WHAT IS THE PROPER SOC DESIGN METHODOLOGY?

Chair: Richard Goering - EE Times, San Jose, CA

Organizer: Stanley Krolikoski

Over the past year two distinct answers have emerged regarding SoC design methodologies. On the one hand, it is posited in the *Reuse Methodology Manual*, that a logic synthesis-based design methodology can be effectively used to develop system chips. An alternative methodology focuses on integration (or "reference") platforms and the customization of the basic application-specific platform through the addition of selected SW and/or HW IP blocks. This panel session will debate the merits of these seemingly incompatible proposed SoC methodologies.

PANEL MEMBERS:

Pierre Bricaud - Mentor Graphics Corp., Sophia Antipolis, France

James Doherty - Integrated Silicon Systems, Belfast, Northern Ireland

Steve Glaser - Cadence Design Systems, Inc., San Jose, CA

Michael Keating - Synopsys, Inc., Mountain View, CA

Stanley J. Krolikoski - Cadence Design Systems, Inc., San Jose, CA

Robert Payne - VLSI Technology, Inc. San Jose, CA

Davoud Samani - Siemens

Semiconductor, Munich, Germany



Friday, June 25

36th DAC full day tutorials

Tutorials will be held at the Ernest N. Morial Convention Center in the Second Level meeting rooms.

8:00 AM - Tutorial Registration Opens (Second Level)

12:00 Noon - Lunch

8:30 AM - Continental Breakfast

5:00 PM - Tutorials End

9:00 AM - Tutorials Begin

Tutorial
One

Rooms
286-287

Automated Layout and Migration in Ultra-Deep Submicron VLSI

Organizer: *Andrew B. Kahng* - Univ. of California, Los Angeles, CA

Presenters:

Cyrus Bamji - Cadence Design Systems, Inc., San Jose, CA

Maarten Berkens - Sagantec, Inc., Eindhoven, The Netherlands

Andrew B. Kahng - Univ. of California, Los Angeles, CA

Chris Strotenberg - Sagantec, Inc., Eindhoven, The Netherlands

Audience: The tutorial is intended for system and circuit designers who would benefit from understanding tool capabilities in this arena, for CAD engineers (both R&D and support), for design project managers, and for academic researchers.

Description: How will the next generation of EDA physical layout tools enable designs to be completed with reasonable effort, while ensuring that not too much performance is left on the table? The central theme of this tutorial is "performance convergence". We will cover important new algorithm techniques and physical design methodologies that will be enabling for high-quality, convergent, automated layout and migration in ultra-deep submicron CMOS. Rather than center on just raw algorithms and equations, the tutorial will convey how optimization and characterization fit within flows and methodologies, including (i) cell-based design in RTL-down methodologies, and (ii) polygon-level design in IP and migration-based flows.

The first section will discuss convergent, high-quality automatic cell-based place-and-route, including state-of-the-art building blocks for cell-based P&R tools (analytic and top-down placement, interconnect topology and routing synthesis), and best practices for layout-aware circuit (device, interconnect) performance optimization for timing, power, and signal integrity. We will also cover approaches to predictable, performance-convergent place-and-route: sizing and wireplanning methodologies, unifications of logical and physical design, and unifications of synthesis and analysis/verification activities.

The second section deals with automated/accelerated custom layout methodology. Topics include: (i) design objectives (area, timing, power, yield, etc.) for which custom-quality layout is needed to recapture performance in ultra-deep submicron; (ii) automated custom block building (e.g., datapath generation and transistor-level layout synthesis methodologies); (iii) basic techniques in polygon compaction; and (iv) tools and methodology to speed up custom layout, including connectivity-driven and constraint assisted design environments, layout-sensitive circuit optimization, and interactions between compaction and optimization.

The third section addresses reuse, migration and optimization of hard layout IP. We begin with the concepts of hard IP reuse, and the appropriate abstractions for use in design characterization and verification (e.g., functional, timing, power, area, etc.). Then we discuss technology trends and their implications, including divergent foundry processes and subwavelength lithography. Finally, we conclude with key issues in layout-level technology migration, including reuse/retargeting within the same technology and issues with analog migration.



Friday, June 25

36th DAC full day tutorials

Tutorial Two

Rooms
291-292

Analog and Mixed-Signal Modeling Using the VHDL-AMS Language

Organizer: *Ernst Christen* - Analogy, Inc., Beaverton, OR

Presenters:

Kenneth Bakalar - Mentor Graphics Corp., Rockville, MD

Ernst Christen - Analogy, Inc., Beaverton, OR

Allen M. Dewey - Duke Univ., Durham, NC

Eduard Moser - Robert Bosch GmbH, Stuttgart, Germany

Audience: The tutorial is intended for VHDL designers who need to incorporate analog effects into their designs, and for analog and mixed-signal designers planning to use the VHDL-AMS language.

Description: The tutorial provides an introduction to modeling of analog and mixed-signal devices using the VHDL-AMS language. VHDL-AMS is a superset of the IEEE Std.1076-1993 VHDL language and has recently been approved as an IEEE standard. Our goal is that at the end of the tutorial the attendees will be able to write portable VHDL-AMS models of moderate complexity and to read and understand any model written in the language. The tutorial consists of two parts.

In the first part we will, after a brief overview of the relevant portions of the VHDL language, introduce the new language elements by describing their purpose and showing their use in practical examples from the following areas: signal flow modeling, systems with conservation semantics (both electrical and non-electrical), mixed analog/digital systems, small-signal AC and noise modeling.

In the second part we shift our focus to practical applications of the VHDL-AMS language, including recommended practices for the use of the language that allow models to be portable across simulation environments. The sample applications include aspects from IC design, mixed-signal modeling at various levels of abstraction, micro-electro-mechanical systems, and a multi-disciplinary (electrical, mechanical, fluidic) system from the automotive industry.

Information Visualization: Creating Advanced Visual Interfaces for Analyzing Designs

Organizer: *Eric Solomon* - Synopsys, Inc., Mountain View, CA

Presenters:

Kevin Mullet - Icarian Inc., Sunnyvale, CA

David Overhauser - Simplex Solutions Inc., Sunnyvale, CA

Eric Solomon - Synopsys, Inc., Mountain View, CA

Audience: This tutorial is intended for CAD tool developers, researchers, circuit designers or engineers who are responsible for developing auxiliary tools to enable design methodologies.

Description: Today's chip designers are faced with the challenge of creating complete systems on a single chip. Much of the designer's time is spent assessing the design's performance characteristics and determining where the problem is when performance falls short of requirements. When trying to resolve timing closure problems, designers are typically forced to wade through pages of textual reports in order to understand the performance characteristics of their design. This form of presentation is very poorly suited to the task of evaluating large quantities of data whose dimensions include spatial arrangement, connectivity, and timing. The complexity of today's designs require the development of abstract visual representations that allow the user of electronic design automation software to interact more directly with the design database in order to more quickly understand the performance characteristics of their design.

Tutorial Three

Rooms
293-294

Tutorial
Three
(cont.)

Powerful mechanisms in human visual perceptual have historically been sadly underutilized in EDA software, but this is beginning to change. Even entry-level workstations are moving steadily in the direction of ever-larger screens with ever-higher resolutions. This trend provides the hardware foundation for software that presents perceptually rich and information abundant displays that allow users to leverage their own highly practiced skills of pattern recognition and perceptual judgment to gain new insight into their design. By dynamically querying the underlying database, users can quickly isolate areas of interest by exploiting the visual interface as a powerful tool for design analysis.

This tutorial provides the background needed to effectively design, assess, or utilize software information visualization systems for electronic design automation. The tutorial describes the principles of visual perception and representation that form the basis for effective visualization of large complex data sets. It surveys successful examples from the information visualization literature, research laboratories and commercial products, and provides an in-depth look at the uses of visualization in EDA software, using examples from leading EDA vendors. One particular focus is on the use of information visualization to helping designers solve timing closure problems. An in-depth example reveals how information visualization is helping today's designer understand the effect of IR drop on clock skew, enabling designers to see how and where their power grid design is having an impact on their chip's performance.

By the end of the day, participants will be able to recognize the essential elements of an effective information visualization system and understand the significance of a number of successful software visualization tools. They will see examples showing current applications of visualization technology in EDA software and get a preview of what to expect in the future based on the most recent laboratory research. All of this information will help participants assess the suitability of information visualization systems for their own design problems and select or develop tools and methodologies that better support their own particular needs.

Tutorial
FourRooms
295-296Overcoming the Technical and Managerial Challenges in
Enabling Design Reuse Within the Engineering Organization

Organizer: *Mike Keating* - Synopsys, Inc., Mountain View, CA

Presenters:

Pierre Bricaud - Mentor Graphics Corp., Sophia Antipolis, France

Warren Savage - Synopsys, Inc., Mountain View, CA

Ulf Schlichtmann - Siemens AG, Munich, Germany

Audience: Engineering Managers and Principal Engineers leading teams designing systems-on-a-chip and semiconductor-IP wanting to implement design reuse practices within their engineering organizations.

Description: This full-day tutorial covers the challenges and benefits in enabling semiconductor design teams to perform effective design reuse. The tutorial is targeted at engineering managers and team leaders trying to enable their engineering teams to do design reuse effectively. The first part of the tutorial will cover rules, design processes and methodologies for creating, verifying, and integrating reusable soft and hard-IP blocks. Design examples are taken from past projects to show the critical factors that enable or prevent IP blocks from being reusable, and the design processes that must be put in place to ensure IP quality. Usage of design tools to create and verify IP blocks and enforce design reuse methodologies will also be covered.

The second part of the tutorial focuses on the managerial and organizational challenges when enabling different product groups within a company to reuse each other's designs. Organizational and process-related barriers will be covered in detail, as well as recommendations for reorganizing design teams and putting in place proper engineering incentives. Material is based on actual experience of Synopsys consultants delivering enterprise-wide design reuse solutions across the semiconductor industry.

Tutorial
FiveRooms
298-299

Embedded Memories in System Design - From Technology to Systems Architecture

Organizer: *Francky Catthoor* - IMEC, Leuven, Belgium

Presenter:

Michael PilsI - Siemens AG, Munich, Germany

Audience: The tutorial is intended for system and architecture designers dealing with systems which include large amounts of memories, and also for (system-level) design tool developers and researchers who look at design methodologies and tools which can support this type of application design.

Description: First, background will be provided on embedded DRAM process, circuit and market issues. The term system-on-silicon has been used to denote the integration of random logic, processor cores, SRAMs, ROMs, and analog components on the same die. But until recently, one major component has been missing: high-density DRAMs. Today's technologies allow the integration of significant amounts of DRAM memory for applications such as data buffering, picture storage, and program/data storage. In quarter-micron technology, chips with up to 128 Mbit of DRAM and 500 k gates of logic are eminently feasible. This enlarges the system design space tremendously since system architects are no longer restricted to standard commodity DRAMs. We will discuss the market for embedded DRAM applications as well as the associated challenges.

Next, the system design requirements from different application domains will be analyzed in session two. The first part will focus on a 32-bit RISC processor with embedded DRAM in the video processing context. It will include the processor micro architecture and organization along with some data on the process technology and design methodology. In a second part, hard-disc-drive (HDD) controllers are addressed, which are a very typical application for an embedded DRAM solution. We will highlight design issues related to such systems on silicon (design flow, required views, HW/SW-codesign, testing aspects). In part three, opportunities, challenges and trends in general-purpose processor architectures for embedded memory systems will be discussed. The focus will be on the recent architectural trends in high-performance microprocessor, including vector, VLIW and reconfigurable architectures, and the IRAM project. We will describe the strengths and disadvantages of each approach in terms of application performance, scalability and design complexity.

The final session will address issues in system design technology and compilation for embedded data-dominated multi-media applications. We will show that decisions made at this stage heavily influence the final outcome when the appropriate architectural issues of the embedded memories are correctly incorporated. We believe much research can be done (and many results are already available) in this new area. We also believe this is an interesting future focus for DAC attendees. Techniques addressed include formal data-flow analysis, reuse and access analysis, the most important memory related data-flow transformations and cache related allocation transformations, techniques for memory estimation, coarse-grain and fine-grain compiler transformations to improve locality, data partitioning and layout schemes, instruction selection and code compression.



Tutorial
Six

Rooms
289-290

Built-In Self-Test for Systems on a Chip

Organizer: *Janusz Rajski* - Mentor Graphics Corp., Wilsonville, OR

Presenters:

Janusz Rajski - Mentor Graphics Corp., Wilsonville, OR

Jerry Tyszer - Poznan Univ. of Technology, Poznan, Poland

Nilanjan Mukherjee - Lucent Technologies, Princeton, NJ

Audience: Designers of complex systems on a chip, ASICs, and ASSPs, IP core providers and integrators, test engineers, researchers, and managers interested in learning about state-of-the-art BIST technology, practices and automation tools.

Description: This tutorial presents state-of-the-art BIST technology, practices and automation tools. It discusses compelling reasons in favor of BIST adoption, i.e., dramatic reduction of test data volume, increased quality of test and reduced manufacturing test cost, in comparison to conventional testing techniques based on stored patterns and test equipment. It also presents common barriers to BIST adoption such as design rules violations, bus conflicts, unknown states propagation to observable outputs, and random pattern resistance.

The tutorial provides a very comprehensive coverage of structured design for testability techniques based on scan, guidelines for design of BIST-able cores, and techniques for random pattern testability. A very detailed presentation of the most popular and effective BIST architectures for random logic covers generators of patterns, compactors of test responses, and controllers. Special emphasis is placed on issues related to at-speed testing and BIST schemes for multi-frequency designs with on-chip generated clocks. Memory BIST presentation focuses on architectures relevant to systems with many embedded memories and shared controllers.

Finally, the tutorial introduces hierarchical BIST methodologies for systems on a chip, based on BIST-ready IP cores and system BIST integration. Automation of BIST synthesis in context of a complete design flow concludes the presentation. All key concepts are illustrated with applications and real industrial case studies. Most complex structures and algorithms are clearly explained with support of multimedia techniques.