



The 38th Design Automation Conference • June 18 - 22, 2001 • Las Vegas, NV

Tuesday, June 19, 2001

8:30
to
10:00

Opening Session and Keynote Speaker (no badge required) **Location: Hilton Pavilion** (Las Vegas Hilton)
Designing in the New Millennium, It's Even Harder Than We Thought
Henry Samueli - Co-Chairman and Chief Technical Officer, Broadcom Corporation, Irvine, CA

BREAK 10:00 - 10:30					
	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 1	Session 2	Session 3	Session 4	Session 5
10:30 to 12:00	PANEL: The Electronics Industry Supply Chain: Who Will do What?	SPECIAL SESSION: Nanometer Futures	System-Level Configurability: Bus Interface and Processor Design	Making Verification More Efficient	SoC and High-Level DFT
LUNCH 12:00 - 2:00					
	Session 6	Session 7	Session 8	Session 9	Session 10
2:00 to 4:00	PANEL: The Next HDL: If C++ is the Answer, What Was the Question?	SPECIAL SESSION: Design for Subwavelength Manufacturability: Impact on EDA	New Ideas in Logic Synthesis	Analog Design and Modeling	Scan-Based Testing
BREAK 4:00 - 4:30					
	Session 11	Session 12	Session 13	Session 14	Session 15
4:30 to 6:00	PANEL: Your Core - My Problem? Integration and Verification of IP	SPECIAL SESSION: Configurable Computing: Reconfiguring the Industry	Interconnect Design Optimization	Power Estimation Techniques	Functional Validation Based on Boolean Reasoning (BDD, SAT)

DAC Cocktail Party at the Las Vegas Convention Center 6:00pm - 7:00pm
Ph.D Forum at the Las Vegas Convention Center 7:00pm - 9:00pm • Room N250

Exhibit Hours 10:00am - 6:00pm / Demo Suite Hours 8:00am - 9:00pm

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.





Presenters will be available in rooms N104 and N118 for additional 20-minute question and answer sessions.

- Videod Session

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Wednesday, June 20, 2001

	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 16	Session 17	Session 18	Session 19	Session 20
8:30 to 10:00	SPECIAL SESSION: Verification: Life Beyond Algorithms	 SPECIAL SESSION: Dissecting an Embedded System: Lessons from Bluetooth	Algorithmic and Compiler Transformations for High-Level Synthesis	Gate Delay Calculation	Memory, Bus and Current Testing
BREAK 10:00 - 10:30					
Plenary Panel					
10:30 to 12:00	 Embedded System Design: The Real Story Room N109-N114 This panel of senior executives, users and providers of embedded systems will examine this burgeoning and increasingly important space.				
LUNCH 12:00 - 2:00					
	Session 21	Session 22	Session 23	Session 24	Session 25
2:00 to 4:00	PANEL: (When) Will FPGAs Kill ASICs?	 SPECIAL SESSION: Inductance 101 and Beyond	Memory Optimization Techniques for DSP Processors	Technology Dependent Logic Synthesis	Collaborative and Distributed Design Frameworks
BREAK 4:00 - 4:30					
	Session 26	Session 27	Session 28	Session 29	Session 30
4:30 to 6:00	PANEL: When Will the Analog Design Flow Catch Up with the Digital Methodology?	 SPECIAL SESSION: Closing the Gap Between ASIC and Custom: Design Examples	Energy and Flexibility Driven Scheduling	Representation and Optimization for Digital Arithmetic Circuits	Techniques for IP Protection

38th DAC • UIVA Las Vegas Party • 7:30pm - 10:30pm • Hilton Center (Las Vegas Hilton)

 - Videod Session

Exhibit Hours 10:00am - 6:00pm / Demo Suite Hours 8:00am - 9:00pm






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Thursday, June 21, 2001

	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 31	Session 32	Session 33	Session 34	Session 35
8:30 to 10:00	 SPECIAL SESSION: Visualization and Animation for VLSI Design	Application-Specific Customization for Systems-on-a-chip	Satisfiability Solvers and Techniques	Power and Interconnect Analysis	Domain Specific Design Methodologies
BREAK 10:00 - 10:30					
	Session 36	Session 37	Session 38	Session 39	Session 40
10:30 to 12:00	 PANEL: Debate: Who Has Nanometer Design under Control?	Analysis and Implementation for Embedded Systems	Industrial Case Studies in Verification	Integrated High-Level Synthesis Based Solutions	Timing Verification and Simulation
 Keynote - FPGAs Enter the Mainstream • 1:00 - 1:45 • Room: N109 - N114 Willem P. Roelandts - President and Chief Executive Officer, Xilinx, Inc.					
	Session 41	Session 42	Session 43	Session 44	Session 45
2:00 to 4:00	 SPECIAL SESSION: On-Chip Communication Architectures	Compiler and Architecture Interactions	Timing with Crosstalk	Low Power Design: Systems to Interconnect	Floorplanning Representations and Placement Algorithms
BREAK 4:00 - 4:30					
	Session 46	Session 47	Session 48	Session 49	Session 50
4:30 to 6:00	 PANEL: What Drives EDA Innovation?	Signal Integrity: Avoidance and Test Techniques	Novel Approaches to Microprocessor Design and Verification	Scheduling Techniques for Power Management	Novel Devices and Yield Optimization

Demo Suite Hours 8:00am - 5:00pm



- Videod Session

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Topics and Related Sessions

If you are interested in the following topics please see the related sessions below.

Embedded Systems:

Sessions: 3, 12, 17, 23, 28, 32, 37, 41, 42, 49 and the Plenary Panel

System Design & Optimization:

Sessions: 3, 6, 12, 21, 25, 35, 41, Tutorial 6

Logic & High Level Synthesis & Optimization:

Sessions: 8, 18, 24, 27, 29, 33, 35, 36, 39, Tutorial 6

Logic & Functional Verification & Simulation:

Sessions: 4, 15, 16, 33, 38, 48

Timing Verification and Simulation:

Sessions: 19, 40, 43

Electrical Modeling & Simulation:

Sessions: 22, 34, 43, 47

Physical Design:

Sessions: 7, 13, 27, 36, 45

Validation & Test:

Sessions: 5, 10, 20, 48, Tutorial 1, Tutorial 4

Impacts of Advancing Technology:

Sessions: 2, 7, 36, Tutorial 4

Device & Interconnect Modeling:

Sessions: 22, 34, 36, 43, 47, 50, Tutorial 2

Analog and Mixed Signal Design:

Sessions: 9, 26, Tutorial 3

Low Power Design:

Sessions: 14, 34, 44, Tutorial 5

Design Re-use, IP and SoC Issues:

Sessions: 4, 11, 30, Tutorial 1

EDA Industry Issues:

Sessions: 1, 12, 46

EDA Methodologies:

Sessions: 25, 31, 35

Tutorials Friday, June 22, 2001

Tutorials will be held at the Las Vegas Convention Center.

8:00 AM - 1:00 PM Tutorial Registration Open 9:00 AM - 5:00 PM Tutorials
8:00 AM - Continental Breakfast 12:00 Noon - Lunch

Tutorial 1 - Design-for-Test Techniques for SoC Designs

ORGANIZER: *Janusz Rajski* - Mentor Graphics Corp., Willsonville, OR

Tutorial 2 - Interactive Tutorial on Fundamentals of Signal Integrity for High-Speed/High-Density Design

ORGANIZERS: *Andreas Cangelaris* - Univ. of Illinois, Urbana, IL
José Schutt-Ainé - Univ. of Illinois, Urbana, IL

Tutorial 3 - CAD Tools for Mixed-Signal and RF ICs

ORGANIZER: *Georges Gielen* - Katholieke Univ., Leuven, Belgium

Tutorial 4 - Design-Manufacturing Interface for UDSM Era: Designer and CAD Tool Developer Perspectives

ORGANIZER: *Andrzej J. Strojwas* - Carnegie Mellon Univ., Pittsburgh, PA

Tutorial 5 - Low Power Tools and Methodologies for the ASIC Industry

ORGANIZER: *Rakesh Patel* - Intel Corp., Santa Clara, CA

Tutorial 6 - Field Programmable Devices: Architecture and CAD Tools

ORGANIZER: *Majid Sarafzadeh* - Univ. of California, Los Angeles, CA

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Opening Session

Location: Hilton Pavilion (Las Vegas Hilton)

Opening Remarks: Jan Rabaey - General Chair, 38th DAC

Awards Presented By: Steven P. Levitan Bing Sheu
ACM/SIGDA Representative IEEE/CAS Representative

Opening Keynote Address: Henry Samueli, Co-Chairman and Chief Technical Officer, Broadcom Corporation, Irvine, CA

Awards/Scholarships

P.O. Pistilli Scholarships (ACSEE)

Scholarships will be awarded to five high school students of under-represented minorities who will be pursuing a degree in Electrical Engineering or Computer Science.

Graduate Scholarships

Scholarships will be awarded to five graduate students to support research in Design Automation.

Student Design Contest Award

An award will be presented to the school sponsoring the best entry to the contest.

Best Paper Awards

Best Paper Awards will be given in the following areas:

1. Design Tools
2. Design Methodology (2)
3. Embedded Systems

Individual Awards

2001 IEEE Fellows
CAD Transactions Best Paper Award
VLSI Transactions Best Paper Award
CAS Industrial Pioneer Award
ACM/SIGDA Distinguished Service Award
Outstanding Young Author Award
Marie R. Pistilli Women in EDA Achievement Award



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S - denotes
short paper

β - denotes
best paper

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Session 1

rm: N111-N114

PANEL: THE ELECTRONICS INDUSTRY SUPPLY CHAIN: WHO WILL DO WHAT?

CHAIR: Rita Glover - EDA Today, Kingman, AZ
ORGANIZER: Rita Glover

The makeup and relationships within the design supply chain are changing rapidly. One-stop shopping, whereby a system house procures most of its design and fabrication services from a single source, is now being supplemented by a host of outsourcing suppliers. These players are developing online integration platforms for outsourced design engineering, business transactions, and data management. This evolution is being felt by the entire design automation industry, whether it be focused on the electronic design for chips, boards, or systems, or even the mechanical design of their packaging and housing. What are the implications of this trend on cost, demand for services, and time to market? How can all parties ride this wave of the future to achieve the best outcome in terms of collaborative design capabilities and quality of results?

PANELISTS:

Rich Becks - Seagate, Longmont, CO
Rick Cassidy - TSMC, San Jose, CA
Marc Halpem - Gartner Group, Inc., Stamford, CT
Henry Jurgens - Celestica, Toronto, ON, Canada
Richard Kubin - Nortel, Research Triangle Park, NC
Ted Vucurevich - Cadence Design Systems, Inc., San Jose, CA

Session 2

rm: N109-N110

SPECIAL SESSION: NANOMETER FUTURES

CHAIR: Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA
ORGANIZERS: Andrew B. Kahng, Kurt Keutzer

This session uncovers the cost and quality landmines that are inherent in the technology roadmap for nanometer silicon — and how the EDA and IC industries must plan to respond. The first talk identifies power as the key challenge to all aspects of quality and performance in nanometer technologies. Power-speed tradeoffs are analyzed at device, circuit and other levels. Leakage is the primary challenge to CMOS scaling, and area/delay/cost penalties may block scaling of today's leakage reduction techniques. Finally, power distribution raises issues regarding the viability of packaging and integration strategies. The second talk examines the consequences of production volumes, time-to-market and manufacturability: How will the billions of dollars to be spent on nanometer fablines affect the design-manufacturing interface? How must IC design respond to the future manufacturing cost structure? And how must IC technology roadmaps themselves adapt to nanometer economic realities?

2.1 Future Performance Challenges in Nanometer Design

Dennis Sylvester, Himanshu Kaul - Univ. of Michigan, Ann Arbor, MI

2.2 IC Design in the High-Cost Nanometer Technologies Era

Wojciech Maly - Carnegie Mellon Univ., Pittsburgh, PA

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Session 3

mm:N115-N117

SYSTEM-LEVEL CONFIGURABILITY: BUS INTERFACE AND PROCESSOR DESIGN

CHAIR: *Pieter van der Wolf* - Philips Research Lab.,
Eindhoven, The Netherlands

ORGANIZERS: *Kees Vissers, Kurt Keutzer*

This session presents technologies that enable and exploit system-level configurability, focusing on system bus networks, interfaces, and configurable processors. The first paper presents a novel high-performance protocol for system buses. The second paper addresses the design of interfaces that enable multi-clock and hybrid synchronous / asynchronous systems. The third paper presents tools for the customization of on-chip bus topologies. The last paper presents an approach for estimating design metrics (area, speed, and power), for a configurable processor IP core.

3.1 LOTTERYBUS: A New High-Performance Communication Architecture for System-on-Chip Designs

Kanishka Lahiri - *Univ. of California at San
Diego, La Jolla, CA*

Anand Raghunathan, Ganesh Lakshminarayana -
NEC Corp., Princeton, NJ

3.2 Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols

Tiberiu Chelcea, Steven M. Nowick - *Columbia
Univ., New York, NY*

3.3S Latency-Driven Design of Multi-Purpose Systems-on-Chip

**Seapahn Meguerdichian, Milenko Drinic, Darko
R. Kirovski** - *Univ. of California, Los Angeles, CA*

3.4S Estimation of Speed, Area, and Power of Parameterizable, Soft IP

Jagesh V. Sanghavi, Albert Wang - *Tensilica,
Inc., Santa Clara, CA*

Session 4

mm: N119-N120

MAKING VERIFICATION MORE EFFICIENT

CHAIR: *Masahiro Fujita* - Univ. of Tokyo, Tokyo, Japan

ORGANIZERS: *Limor Fix, Timothy Kam*

With the current limitation in capacity and runtime, verification can be a bottleneck in a design flow. The research presented in this session targets improving the efficiency of verification. The first paper employs multiple engines including BDD-ATPG and 3-value simulation. A novel microprocessor architecture is verified with the proposed design-for-verifiability technique in the second paper. The third paper proposed how various verilog RTL constructs can be symbolically simulated.

4.1 Formal Property Verification by Abstraction Refinement with Formal Simulation and Hybrid Engines

Dong Wang - *Carnegie Mellon Univ., Pittsburgh, PA*

Pei-Hsin Ho, Jiang Long, James Kukula -
Synopsys, Inc., Beaverton, OR

Yunshan Zhu, Tony Ma - *Synopsys, Inc.,
Mountain View, CA,*

Robert Damiano - *Synopsys, Inc., Beaverton, OR*

4.2 Scalable Hybrid Verification of Complex Microprocessors

**Maher N. Mneimneh, Fadi A. Aloul, Saugata
Chatterjee, Chris Weaver, Kareem A. Sakallah,
Todd Austin** - *Univ. of Michigan, Ann Arbor, MI*

4.3 Symbolic RTL Simulation

Alfred Koelbl - *Technical Univ. of Munich,
Munich, Germany*

James Kukula, Robert Damiano - *Synopsys, Inc.,
Beaverton, OR*

Session 5

mm: N107-N108

SoC AND HIGH-LEVEL DFT

CHAIR: *Yervant Zorian* - *LogicVision, Inc., San Jose, CA*

ORGANIZERS: *Anand Raghunathan, Iith Pomeranz*

This session starts with a paper addressing issues related to the VSIA/IEEE P1500 standard for SoC testing. The second paper deals with instruction-level DFT to support self-testing of SoC with processor cores. The third paper proposes a BIST-based DFT methodology using RTL testability analysis.

5.1 A Unified DFT Architecture for Use with IEEE 1149.1 and VSIA/IEEE P1500 Compliant to Test Access Controllers

Bulent I. Dervisoglu - *Cadence Design Systems,
Inc., San Jose, CA*

5.2 Instruction-Level DFT for Testing Processor and IP Cores in System-on-a-Chip

WeiCheng Lai, Tim Cheng - *Univ. of California,
Santa Barbara, CA*

5.3 Test Strategies for BIST at the Algorithmic and Register-Transfer Levels

Kelly Ockunzzi - *IBM Corp., Burlington, VT*
Chris Papachristou - *Case Western Reserve Univ.,
Cleveland, OH*



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S – denotes
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Session 6

rm: N111-N114

PANEL: THE NEXT HDL: IF C++ IS THE ANSWER, WHAT WAS THE QUESTION?

CHAIR: Rajesh K. Gupta - Univ. of California, Irvine, CA
ORGANIZER: Shishpal Rawat

The focus of this panel is on issues surrounding use of C++ in modeling and the integration of silicon IP and system-on-chip designs. In the last two years there have been several announcements promoting C++ based solutions and of multiple consortia (SystemC, Cynapps, Accellera, SpecC) that represent increasing commercial interest both from tool vendors as well as perhaps expression of genuine needs from design houses. There are, however, serious questions about what value proposition a C++ based design methodology brings to the IC or system designer? What has changed in the modeling technology (and/or available tools) that gives a new capability? Is synthesis the right target? or Validation? Tester modeling or testbench generation? This panel brings together advocates and opponents from the design houses and tool developers to highlight the modeling advances.

PANELISTS:

Gérard Beny - Esterel Technologies,
Villeneuve-Loubet, France

Ramesh Chandra - ST Microelectronics, San Diego, CA

Daniel Gajski - Univ. of California, Irvine, CA

Kris Konigsfeld - Intel Corp., Hillsboro, OR

Patrick Schaumont - IMEC, Leuven, Belgium

Ingrid Verbaauwhede - Univ. of California,
Los Angeles, CA

Session 7

rm: N109-N110

SPECIAL SESSION: DESIGN FOR SUBWAVELENGTH MANUFACTURABILITY: IMPACT ON EDA

CHAIR: Robert C. Pack - Cadence Design Systems, Inc., San Jose, CA
ORGANIZERS: Lars Liebman, Andrew B. Kahng

Minimum feature sizes that are much smaller than stepper wavelengths stress the design flow and the design-manufacturing interface as never before. Already, optical proximity correction (OPC), phase-shifting masks (PSM), and pattern density control break traditional flows and reuse paradigms, and dramatically increase design cost. How must EDA change to meet this challenge? The first two papers present experiences and cost-benefit analysis of IDMs who have developed and deployed complete layout and verification methodologies at 150nm and below. The next three papers describe vendor experiences with OPC- and PSM-enabling tools and methodologies. The session will conclude with open Q&A for all presenters.

7.1 Reticle Enhancement Technology: Implications and Challenges for Physical Design

Warren Grobman, Ruoping Wang, Ruiqi Tian, Ertugrul Demircan, Matt Thompson, Chi-Min Yuan - *Motorola DigitalDNA Labs., Austin, TX*

7.2 Enabling Alternating Phase Shifted Mask Designs for a Full Logic Gate Level: Design Rules and Design Rule Checking

Lars Liebmann - *IBM Microelectronics, Hopewell Junction, NY*
Jennifer Lund, Fook-Luen Heng - *IBM Corp., Yorktown Heights, NY*
Ioana Graur - *IBM Microelectronics, Hopewell Junction, NY*

7.3S Layout Design Methodologies for Sub-Wavelength Manufacturing

Michael L. Rieger, Jeffrey P. Mayhew - *Avant! Corp., Beaverton, OR*
Sridhar Panchapakesan - *Avant! Corp., Fremont, CA*

7.4S Production Adoption of OPC and the Impact on Design and Layout

F. M. Schellenberg, N. Cobb, Y. Granik - *Mentor Graphics Corp., San Jose, CA*
L. Capodiecchi, R. Socha - *ASML MaskTools, Santa Clara, CA*

7.5S A Practical Application of Full-Feature Alternating Phase-Shifting Technology for a Phase-Aware Standard-Cell Design Flow

Michel Cote, Philippe Hurat, Vinod Malhotra, **Michael Sanie** - *Numerical Technologies, Inc., San Jose, CA*

7.6S Open Session for Q & A

Session 8

rm: N115-N117

NEW IDEAS IN LOGIC SYNTHESIS

CHAIR: Yusuke Matsunaga - Fujitsu Labs. Ltd.,
Kawasaki, Japan

ORGANIZERS: Timothy Kam, Masahiro Fujita

The first paper introduces a new logic synthesis technique considering reliability issues of LSI. The remaining three papers discuss new algorithms in combinational logic synthesis targeting decomposition of incompletely specified logic functions, factoring of read-once functions, and logic synthesis with exclusive-or gates.

8.1 Layout-Driven Hot-Carrier Degradation Minimization Using Logic Restructuring Techniques

Chih-Wei (Jim) Chang, Kai Wang, Malgorzata Marek-Sadowska - Univ. of California, Santa Barbara, CA

8.2 An Algorithm for Bi-Decomposition of Logic Functions

Alan Mishchenko - Portland State Univ., Portland, OR
Bernd Steinbach - Freiberg Univ. of Mining and Technology, Freiberg, Germany
Marek Perkowski - Portland State Univ., Portland, OR

8.3 Factoring and Recognition of Read-Once Functions Using Cographs and Normality

Martin C. Golumbic, Aviad Mintz - Bar Ilan Univ., Ramat Gan, Israel
Udi Rotics - Netanya Academic College, Netanya, Israel

8.4 Logic Minimization Using Exclusive OR Gates

Valentina Ciriani - Univ. di Pisa, Pisa, Italy

Session 9

rm: N119-N120

ANALOG DESIGN AND MODELING

CHAIR: Alper Demir - CelLight, Inc., Springfield, NJ
ORGANIZERS: Joel Phillips, Noel Menezes

The first paper in this session presents a working design of a high-speed clock and data recovery circuit for optical networking applications. The remaining papers describe progress in a collection of analog CAD topics — stochastic analysis of data converters, partitioning of mixed-signal designs, and efficient analog symbolic analysis.

9.1 Student Design Contest: Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems

Jafar Savoj, Behzad Razavi - Univ. of California, Los Angeles, CA

9.2 A Novel Method for Stochastic Nonlinearity Analysis of a CMOS Pipeline ADC

David Goren, Israel A. Wagner, Elyahu Shamsaev - IBM Corp., Haifa, Israel

9.3 Behavioral Partitioning in the Synthesis of Mixed Analog-Digital Systems

Sree Ganesan, Ranga Vemuri - Univ. of Cincinnati, Cincinnati, OH

9.4 Efficient DDD-Based Symbolic Analysis of Large Analog Circuits

Wim Verhaegen, Georges G. Gielen - Katholieke Univ., Leuven, Belgium

Session 10

rm: N107-N108

SCAN-BASED TESTING

CHAIR: T. M. Mak - Intel Corp., Santa Clara, CA
ORGANIZERS: Anand Raghunathan, Tim Cheng

This session deals with issues related to fault coverage improvement, test volume and test time reduction for scan-based designs. The first paper uses limited scan operations to improve random pattern fault coverage. The next three papers describe different compaction techniques. The last paper deals with a compression technique for test data and power reduction.

10.1 Random Limited-Scan to Improve Random Pattern Testing of Scan Circuits

Irit Pomeranz - Purdue Univ., West Lafayette, IN

10.2 Test Volume and Application Time Reduction Through Scan Chain Concealment

Ismet Bayraktaroglu, Alex Orailoglu - Univ. of California at San Diego, La Jolla, CA

10.3 An Approach to Test Compaction for Scan Circuits that Enhances At-Speed Testing

Irit Pomeranz - Purdue Univ., West Lafayette, IN
Sudhakar M. Reddy - Univ. of Iowa, Iowa City, IA

10.4S Generating Efficient Tests for Continuous Scan

Sying Jyan Wang, Sheng Nan Chiou - National Chung-Hsing Univ., Taichung, Taiwan, ROC

10.5S Combining Low-Power Scan Testing and Test Data Compression for System-on-a-Chip

Anshuman Chandra, Krishnendu Chakrabarty - Duke Univ., Durham, NC



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Session 11

rm: N111-N114

PANEL: YOUR CORE - MY PROBLEM? INTEGRATION AND VERIFICATION OF IP

CHAIR: Gabe Moretti - EDN Magazine, Niwot, CO

ORGANIZERS: Nanette Collins, Gabe Moretti, Dave Kelf

As the popularity of reusing existing designs — or Intellectual Property (IP) — continues to grow, design challenges escalate. The most time-consuming and critical part of IP design and reuse is verifying that it will work as designed and as the user intends. Designers are pushing the limits of IP for new, distinctive and innovative applications. With this innovation comes problems that will need creative solutions. Product verification, for example, will become more and more important in ensuring the correctness of designs. Over the years, various solutions have come on the market, all seemingly useful, but none reducing the time or manpower it takes to verify a design. With designs becoming increasingly more complex with each new project and verification consuming up to 70% of a design cycle, something must be done to alleviate the bottleneck. The panel will look at various alternatives for IP verification today, including universal simulation, hardware acceleration, formal verification, and semi-formal verification. Panelists, who are experienced designers and representatives of organizations offering EDA tools to beat the verification bottleneck will work toward identifying the methodology best suited for IP design.

PANELISTS:

Tom Anderson - 0-In Design Automation, San Jose, CA

Janick Bergeron - Qualis Design Corp., Lake Oswego, OR

Ashish Dixit - Tensilica, Inc., Santa Clara, CA

Peter Flake - Co-Design Automation, Inc., Los Altos, CA

Tim Hopes - ARM, Maidenhead, UK

Ramesh Narayanaswamy - Tharas Systems Inc., Santa Clara, CA

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Session 12

rm: N109-N110

SPECIAL SESSION: CONFIGURABLE COMPUTING: RECONFIGURING THE INDUSTRY

CHAIR: Diederik Verkest - IMEC, Leuven, Belgium

ORGANIZERS: Diederik Verkest, Kurt Keutzer

Cost effective systems use specialization to optimize factors such as power consumption, processing throughput, flexibility, or combinations thereof. Reconfiguration has been proposed as a mechanism to create run-time specialization. This session will address the concept of reconfiguration at different hierarchical levels, the architectural aspects of reconfigurable computing, the link between application domain and reconfigurability needs, and the design techniques supporting reconfiguration.

12.1 A Quick Safari through the Reconfiguration Jungle

Patrick Schaumont - IMEC, Leuven, Belgium

Ingrid Verbauwhede - Univ. of California, Los Angeles, CA

Kurt Keutzer - Univ. of California, Berkeley, CA

Majid Sarafzadeh - Univ. of California, Los Angeles, CA

12.2 ReConfigurable Computing in Wireless

Bill Salefski, Levent Caglar - Chameleon Systems, Inc., San Jose, CA

12.3 Hardware/Software Instruction Set Configurability for System-on-Chip Processors

Albert Wang, Chris Rowen, Dror Mayden, Earl Killian - Tensilica, Inc., Santa Clara, CA

Session 13

rm: N115-N117

INTERCONNECT DESIGN OPTIMIZATION

CHAIR: *Martin D. F. Wong - Univ. of Texas, Austin, TX*

ORGANIZERS: *Jason Cong, Louis Scheffer,
Patrick Groeneveld*

This session presents various approaches to the design and planning of interconnect. The first two papers deal with global wiring optimization, while the third paper addresses the crosstalk minimization problem. The final paper presents new results on optimal switchbox interconnect design for FPGAs.

β 13.1 A Practical Methodology for Early Buffer and Wire Resource Allocation

Charles J. Alpert, Jiang Hu - IBM Austin Research Lab., Austin, TX

Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

Paul G. Villarubia - IBM Corp., Austin, TX

13.2S Creating and Exploiting Flexibility in Steiner Trees

Elaheh Bozorgzadeh, Ryan Kastner, Majid Sarafzadeh - Univ. of California, Los Angeles, CA

13.3S Simultaneous Shield Insertion and Net Ordering for Coupled RLC Nets Under Explicit Noise Constraint

Kevin Lepak, Irwan Luwandi, Lei He - Univ. of Wisconsin, Madison, WI

13.4 On Optimum Switch Box Designs for 2-D FPGAs

Hongbing Fan - Univ. of Victoria, Victoria, BC, Canada

Jiping Liu - Univ. of Lethbridge, Lethbridge, AB, Canada

Yu Liang Wu, Chak Chung Cheung - Chinese Univ. of Hong Kong, Hong Kong, China

Session 14

rm: N119-N120

POWER ESTIMATION TECHNIQUES

CHAIR: *Massoud Pedram - Univ. of Southern California, Los Angeles, CA*

ORGANIZERS: *Donatella Sciuto, Kazutoshi Wakabayashi*

The first two papers of the session introduce two models for evaluating power consumption in combinational circuits. The first paper estimates switching activities by capturing complex dependencies among signals using probabilistic techniques. The second paper deals with power sensitivity estimation of a presynthesized circuit. Finally, the third paper considers a different level of abstraction by presenting a software energy estimation methodology considering current consumption.

14.1 Dependency Preserving Probabilistic Modeling of Switching Activity Using Bayesian Networks

Sanjukta Bhanja, Nagarajan Ranganathan - Univ. of South Florida, Tampa, FL

14.2 A Static Estimation Technique of Power Sensitivity in Logic Circuit

Taewhan Kim - KAIST, Taejeon, Korea

Kiseok Chung - Intel Corp., Santa Clara, CA

C. L. Liu - National Tsing-Hua Univ., Hsinchu, Taiwan, ROC

14.3 JouleTrack - A Web Based Tool for Software Energy Profiling

Amit Sinha, Anantha P. Chandrakasan - Massachusetts Institute of Tech., Cambridge, MA

Session 15

rm: N107-N108

FUNCTIONAL VALIDATION BASED ON BOOLEAN REASONING (BDD, SAT)

CHAIR: *Limor Fix - Intel Semiconductors Ltd., Haifa, Israel*

ORGANIZERS: *Masahiro Fujita, Timothy Kam*

Many tasks in EDA, such as equivalence checking, property checking, logic synthesis, and false path analysis are based on Boolean Function analysis using BDD Technology and SAT solvers. In this session, state of the art SAT solvers will be presented. The benefit of circuit information for optimizing SAT and BDD will be discussed, and the use of symbolic simulation for partial equivalence checking will be demonstrated.

15.1 Effective Use of Boolean Satisfiability Procedures in the Formal Verification of Superscaler and ULIW Microprocessors

Miroslav N. Velev, Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

15.2 Circuit-Based Boolean Reasoning

Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA

Malay K. Ganai - Univ. of Texas, Austin, TX

Viresh Paruthi - IBM Corp., Austin, TX

15.3 Checking Equivalence for Partial Implementations

Christoph Scholl, Bernd Becker - Univ. of Freiburg, Freiburg, Germany



Wednesday
June 20

8:30
to
10:00

All speakers are
denoted in bold

S - denotes
short paper

β - denotes
best paper

18

Session 16

rm: N111-N114

SPECIAL SESSION: VERIFICATION: LIFE BEYOND ALGORITHMS

CHAIR: Carl Pixley - Motorola, Inc., Austin, TX
ORGANIZER: Carl Pixley

The speakers will address the nuts and bolts of commercial verification projects, describing the various techniques used, the resources required and the effectiveness of different techniques. The general education of engineers in verification is addressed in the final paper.

16.1 Validating the Intel® Pentium® 4 Microprocessor

Bob Bentley - Intel Corp., Hillsboro, OR

16.2 Nuts and Bolts of Core and SoC Verification

Ken Albin - Motorola, Inc., Austin, TX

16.3 Teaching Future Verification Engineers - The Forgotten Side of Logic Development

Bruce Wile - IBM Corp., Poughkeepsie, NY

Fusun Ozguner, Duane Marhefka - Ohio State Univ.,
Columbus, OH

Lyle Hanrahan - IBM Corp., Rochester, MN

Jennifer Stofer - IBM Corp., Austin, TX

Joanne De Groat - Ohio State Univ., Columbus OH

Session 17

rm: N109-N110

SPECIAL SESSION: DISSECTING AN EMBEDDED SYSTEM: LESSONS FROM BLUETOOTH

CHAIR: Jan Rabaey - Univ. of California, Berkeley, CA
ORGANIZERS: Jan Rabaey, Anantha Chandrakasan

Ad-hoc wireless networking based on the Bluetooth Standard is one of the hottest topics in wireless today. The design process and methodology of a leading-edge bluetooth chip set will be presented and analyzed. The tough specifications of Bluetooth and its complexity necessitate advanced design verification and test techniques, which are the focus of this session.

17.1 SoC Integration of Reusable Baseband Bluetooth IP

Barry Clark, Torbjöm Graham- Ericsson Tech. Licensing AB,
Lund, Sweden

17.2 One-Chip Bluetooth ASIC Challenges

Paul van Zeijl - Ericsson EuroLab., Emmen, The Netherlands

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 18

rm: N115-N117

ALGORITHMIC AND COMPILER TRANSFORMATIONS FOR HIGH-LEVEL SYNTHESIS

CHAIR: Hiroto Yasuura - Kyushu Univ., Fukuoka, Japan

ORGANIZERS: Kazutoshi Wakabayashi, Rajesh K. Gupta

The quality of synthesized circuits is a major concern for many high-level synthesis solutions. This session addresses techniques that work with HLS algorithms to improve synthesis results. The first paper presents global transformations for controller synthesis. The second and third papers examine techniques using parallelizing compilers that directly effect HLS solutions. The last paper examines arithmetic-level optimizations.

18.1 Transformations for the Synthesis and Optimization of Asynchronous Distributed Control

Michael Theobald, Steven M. Nowick - Columbia Univ., New York, NY

18.2S Speculation Techniques for High Level Synthesis of Control Intensive Designs

Sumit Gupta, Nick O. Savoie, Sunwoo Kim, Nikil Dutt, Rajesh K. Gupta, Alexandru Nicolau - Univ. of California, Irvine, CA

18.3S Parallelizing DSP Nested Loops on Reconfigurable Architectures Using Data Context Switching

Kiran K. Bondalapati - Univ. of Southern California, Los Angeles, CA

18.4 Using Symbolic Algebra in Algorithmic Level DSP Synthesis

Armita Peymandoust, Giovanni De Micheli - Stanford Univ., Stanford, CA

Session 19

rm: N119-N120

GATE DELAY CALCULATION

CHAIR: Satya Pallela - eSilicon Corp., Allentown, PA

ORGANIZERS: Jaijeet Roychowdhury, Joel Phillips

This session has three papers on gate delay calculation. The first paper uses BDDs to quickly explore the space of switching transitions, enabling accurate delay simulation of only a few sets of transitions. The second paper derives an empirical delay model for a NAND gate, accounting for simultaneous switching and relative input positions, and outlines applications to timing analysis and incremental timing refinement. The third paper analyzes the effect of power supply variations on gate delay with three techniques, obtaining increasingly tight upper bounds on worst-case delay.

19.1 Computing Logic-Stage Delays Using Circuit Simulation and Symbolic Elmore Analysis

Clayton B. McDonald, Randal E. Bryant - Carnegie Mellon Univ., Pittsburgh, PA

19.2 A New Gate Delay Model for Simultaneous Switching and Its Applications

Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer - Univ. of Southern California, Los Angeles, CA

19.3 Static Timing Analysis Including Power Supply Noise Effect on Propagation Delay in ULSI Circuit

Geng Bai, Sudhakar Bobba, Ibrahim N. Hajj - Univ. of Illinois, Urbana, IL

Session 20

rm: N107-N108

MEMORY, BUS AND CURRENT TESTING

CHAIR: Magdy S. Abadir - Motorola, Inc., Austin, TX

ORGANIZERS: Irith Pomeranz, Tim Cheng

This session includes a paper on test generation and test scheduling for multiport memories, papers on bus testing and a paper on fault characterization and DFT for CMOS/BiCMOS circuits. In the area of bus testing, the papers cover IDDT testing and the use of embedded processor cores for interconnect crosstalk defects.

20.1 Simulation-Based Test Algorithm Generation and Port Scheduling for Multi-Port Memories

ChiFeng Wu, ChihTsun Huang, KuoLiang Cheng, ChihWea Wang, ChengWen Wu - National Tsing-Hua Univ., Hsinchu, Taiwan, ROC

β 20.2 Improving Bus Test Via IDDT and Boundary Scan

Shi-yu Yang - Intel Corp., Hillsboro, OR
Chris Papachristou, Massood Tabib-Azar - Case Western Reserve Univ., Cleveland, OH

20.3S Fault Characterizations and Design-for-Testability Technique for Detecting IDDQ Faults in CMOS/BiCMOS Circuits

Kaamran Raahemifar - Ryerson Polytechnic Univ., Toronto, ON, Canada
Majid Ahmadi - Univ. of Windsor, Windsor, ON, Canada

20.4S Testing for Interconnect Crosstalk Defects Using On-Chip Embedded Processor Cores

Li Chen, Xiaoliang Ba, Sujit Dey - Univ. of California at San Diego, La Jolla, CA



Wednesday
June 20

10:30
to
12:00

All speakers are
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S - denotes
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20

PLENARY PANEL

EMBEDDED SYSTEM DESIGN: THE REAL STORY

rm: N109-N114

CHAIR: *Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA*

ORGANIZERS: *Randy Harr, Wayne Wolf*

PRESENTERS: *Augusto de Oliveira - Philips Semiconductor, Sunnyvale, CA* *Jim Ready - MontaVista Software, Sunnyvale, CA*
Roger Fordham - Motorola, Inc., Schaumburg, IL *Fabio Romeo - Magneti Marelli, Torino, Italy*
Mark Pinto - Agere Systems, Allentown, PA

Description: Every object in common use tomorrow will have an electronic component that, we hope, will enhance its functionality, its reliability, and its safety. An automobile, a cellular phone, and a home are already complex electronic systems and will become more so. The billion-transistor ASIC complexity that has been touted as the challenge for methodologies and EDA does pale in comparison when mixed with the complexity of embedded systems. Embedded systems are heterogeneous, they are connected to networks, they have multiple and conflicting requirements of cost, performance, functionality, safety, and time to market. Being late to the market for just a few weeks may mean the loss of hundreds of millions of dollars, but being wrong can be tragic.

The entire electronics industry has been restructuring to face the challenges of embedded system design and production. Less frequently are such designs carried out by a single company. With outsourcing of both design and manufacturing, each contributor focuses on its core competency. Hence, the interfaces among system, IP providers, semiconductor-design companies and manufacturing companies are becoming the pivotal points to understand for the future of the electronics industry.

Several ideas are emerging to cope with complexity, time-to-market and cost of designing these pervasive embedded systems and their integrated circuits. Platform-based design, for example, has become an important design style and, if well implemented, is essential to providing reuse of software and hardware components over two or more possibly disparate design projects as well as a clean interface among system, IP and semiconductor companies. Since the flexibility

of a platform is strictly connected to the re-usability of the programmable and reconfigurable parts, reusable software design, crystal ball architecture selection and complex configuration methods are becoming essential ingredients of embedded system design. Embedded software traditionally has had different characteristics when compared with traditional large software systems encountered in data base applications and computer systems. Real-time reactions to the environment and complex signal processing are typical for most applications of embedded systems such as cellular phones and engine controllers. The real-time requirements pose the most interesting challenges to embedded software design. Indeed the choice of implementation of a function as a hardware module or a software program is the result of trade-offs involving time-to-market, power consumption, performance and cost.

The participants in this panel are among the key enablers of the new embedded system design frontier and will address:

- The issues associated with critical markets now dependent upon embedded systems: automotive, cellular and consumer electronics.
- The embedded software design challenges and trends in view of the latest research and industrial offerings.
- Platform-based design as an effective way of reducing risk and complexity of the overall design process as well as sustaining the electronics supply chain.

Alberto L. Sangiovanni-Vincentelli

Alberto Sangiovanni-Vincentelli is Professor of Electrical Engineering and Computer Sciences at the University of California at Berkeley, where he serves on the Advisory Board of the Lester Center of the Haas School of Business and of the Center for Western European Studies, and is a member of the Berkeley Roundtable of the International Economy. He is a co-founder of Cadence and Synopsys and serves on the boards of a variety of new and established companies. He is author of over 500 papers and eleven books, and is a Fellow of the IEEE and a Member of the National Academy of Engineering.

Augusto de Oliveira

Augusto de Oliveira is currently Chief Architect for the Consumer Systems Business Unit of Philips Semiconductors, responsible for digital video platform software and hardware architectures. He previously held technical and management positions with Philips in Brazil, The Netherlands and the United States, including manager of the Philips MIPS Technology Center and CTO and Systems Development Manager for the Handheld Computing Group. He has also worked at Philips Research and Philips Business Communications.

Roger Fordham

Roger Fordham is Director of Performance Excellence for the Motorola Global Software Group and has the responsibility for advanced software development environments for Motorola's communications businesses and for establishing the software business and engineering culture and development environment in software development centers worldwide. He has worked for Motorola on four continents, establishing and directing the company's software development business and lecturing on software development, engineering, and culture. He is a Fellow of the Institute of Engineers Australia and has been active in national and international software engineering standards activities and educational endeavors.

Mark Pinto

Mark Pinto is Chief Technical Officer of Agere Systems, formerly the Microelectronics Group of Lucent Technologies and is responsible for technology strategy and research activities in electronic and optoelectronic devices, integrated circuit design, and software and systems. He is also Vice President of Platform Technologies, leading the company's efforts to deliver system-on-a-chip hardware cores, communications software elements, development software, methodologies, tools, models and analysis. He has authored more than 150 journal and professional conference papers and has eight patents in semiconductor devices. He is a Fellow of the IEEE.

Jim Ready

Jim Ready is founder, President and CEO of MontaVista Software, which provides the Linux operating system to the embedded systems market through its Hard Hat Linux flagship product, and offers embedded systems expertise to the open source Linux community. He was co-founder and president of Ready Systems, which developed the first commercially viable real time operating system product, and CTO of its successor, Microtec Research, which was later acquired by Mentor Graphics. He has over 25 years of technical and entrepreneurial experience and is a recognized authority in the embedded systems and real-time software industry.

Fabio Romeo

Fabio Romeo is Executive Vice President of Magneti-Marelli, and President and General Manager of the Electronic System Division, which manufactures electronic products for the corporation and develops dashboard and infotelematics products. He previously held positions at Politecnico di Milano and at Honeywell Information Systems, Italy. He has been active in the development of embedded systems for automotive applications, particularly in the definition of design methodologies necessary to guarantee reduced time-to-market, hardware-software independence, and increased quality levels in software and hardware.



Wednesday
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2:00
to
4:00

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S - denotes
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best paper

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Session 21

rm: N111-N114

PANEL: (WHEN) WILL FPGAS KILL ASICS?

CHAIR: Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

ORGANIZER: Rob A. Rutenbar

There was a time in the dim historical past when foundries actually made ASICs with only 5000 to 50,000 logic gates. But FPGAs and CPLDs conquered those markets and pushed ASIC silicon toward opportunities with more logic, volume, and speed. Today's largest FPGAs approach the few-million-gate size of a typical ASIC design, and continue to sprout embedded cores, such as CPUs, memories, and interfaces. And given the risks of non-working nanometer silicon, FPGA costs and time-to-market are looking awfully attractive. So, will FPGAs kill ASICs? ASIC technologists certainly think not. ASICs are themselves sprouting patches of programmable FPGA fabric, and pushing new realms of size and especially speed. New tools claim to have tamed the convergence problems of older ASIC flows. Is the future to be found in a market full of FPGAs with ASIC-like cores? ASICs with FPGA cores? Other exotic hybrids? Our panelists will share their disagreements on these prognostications.

PANELISTS:

Max Baron - *Microprocessor Report, Sunnyvale, CA*

Thomas Daniel - *LSI Logic Corp., Milpitas, CA*

Rajeev Jayaraman - *Xilinx, Inc., San Jose, CA*

Zvi Or-Bach - *eASIC, San Jose, CA*

Jonathan Rose - *Altera Corp., Univ. of Toronto,
Toronto, ON, Canada*

Carl Sechen - *Univ. of Washington, Seattle, WA*

Session 22

rm: N109-N110

SPECIAL SESSION: INDUCTANCE 101 AND BEYOND

CHAIR: Phillip Restle - *IBM Corp., TJ Watson Research Ctr.,
Yorktown Heights, NY*

ORGANIZERS: Joel Phillips, Noel Menezes

Inductance issues create new signal integrity and delay problems for multigigahertz designs. A basic introduction to the cause and effect of inductance in VLSI circuits is presented along with an industry approach to handling inductance effects in designs. Two final papers present strategies for on-chip inductance modeling.

22.1 Inductance 101: Modeling and Extraction

Michael W. Beattie, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

22.2 Inductance 101: Analysis and Design Issues

Kaushik Gala, David Blaauw, Junfeng Wang,
Vladimir Zolotov, Min Zhao - *Motorola, Inc., Austin, TX*

22.3 Modeling Magnetic Coupling for On-Chip Interconnect

Michael W. Beattie, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

22.4 Min/Max On-Chip Inductance Models and Delay Metrics

Yi Chang Lu - *Stanford Univ., Stanford, CA*
Mustafa Celik, Tak Young - *Monterey Design Inc., Sunnyvale, CA*
Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 23

rm: N115-N117

MEMORY OPTIMIZATION TECHNIQUES FOR DSP PROCESSORS

CHAIR: Daniel Connors - Univ. of Colorado, Boulder, CO
ORGANIZERS: Dirk Grunwald, Marco Di Natale

These papers describe mechanisms to reduce memory size or bandwidth for embedded applications. The first paper presents compiler algorithms to exploit multiword memory transfer. The second shows how to reduce address register changes for common DSPs and the last two papers show how to automatically reduce the total memory needed by applications.

23.1 Utilizing Memory Bandwidth in DSP Embedded Processors

Catherine H. Gebotys - Univ. of Waterloo,
Waterloo, ON, Canada

23.2 Address Code Generation for Digital Signal Processors

Sathishkumar Udayanarayanan, Chaitali
Chakrabarti - Arizona State Univ., Tempe, AZ

23.3 Reducing Memory Requirements of Nested Loops for Embedded Systems

J. Ramanujam, Jinpyo Hong - Louisiana State
Univ., Baton Rouge, LA
Mahmut Kandemir - Penn State Univ.,
University Park, PA
Ashish Narayan - Louisiana State Univ.,
Baton Rouge, LA

23.4 Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications

Per G. Kjeldsberg - Norwegian Univ. of Science
and Tech., Trondheim, Norway
Francky Cathoor - MEC, Leuven, Belgium
Einar J. Aas - Norwegian Univ. of Science and
Tech., Trondheim, Norway

Session 24

rm: N119-N120

TECHNOLOGY DEPENDENT LOGIC SYNTHESIS

CHAIR: Peichen Pan - APLUS Design Technologies, Inc.,
Los Angeles, CA

ORGANIZERS: Jason Cong, Malgorzata Marek-Sadowska

This session introduces us to power problems in technology dependent synthesis. The first paper describes an idea to speed up structural mapping. The second paper introduces some of the issues of incorporating domino circuitry in technology mapping. Latch and latency control and optimization during wave steering is the topic of the third paper. Paper four describes the problem of two level clustering in the context of FPGA synthesis.

24.1 A New Structural Pattern Matching Algorithm for Technology Mapping

Min Zhao - Motorola, Inc., Austin, TX
Sachin S. Sapatnekar - Univ. of Minnesota,
Minneapolis, MN

24.2 Technology Mapping for SOI Domino Logic Incorporating Solutions for the Parasitic Bipolar Effect

Srirang K. Karandikar, Sachin S. Sapatnekar -
Univ. of Minnesota, Minneapolis, MN

24.3 Latency and Latch Count Minimization in Wave Steered Circuits

Amit Singh, Arindam Mukherjee, Malgorzata
Marek-Sadowska - Univ. of California,
Santa Barbara, CA

24.4 Performance-Driven Multi-Level Clustering with Application to Hierarchical FPGA Mapping

Jason Cong, Michail Romesis - Univ. of
California, Los Angeles, CA

Session 25

rm: N107-N108

COLLABORATIVE AND DISTRIBUTED DESIGN FRAMEWORKS

CHAIR: Satish Venkatesan - Intel Corp., Santa Clara, CA
ORGANIZERS: Noel Menezes, Vivek Tiwari

The use of collaborative frameworks for expediting design tasks is receiving increased attention due to the increasing complexity of current ICs. The first paper deals with a novel approach to design process management while the second paper presents a universal client with a user-configurable GUI for distributed design. A collaborative framework for training and design, and an object-oriented framework for specification and synthesis are described in the final papers.

25.1 Application of Constraint-Based Heuristics in Collaborative Design

Juan Antonio Carballo - IBM Austin Research
Lab., Austin, TX
Stephen W. Director - Univ. of Michigan,
Ann Arbor, MI

25.2 A Universal Client for Distributed Networked Design and Computing

Franco Brglez, Hemang Lavana - N. Carolina
State Univ., Raleigh, NC

25.3 Hypermedia-Aided Design

Darko R. Kirovski, Miodrag Potkonjak, Milenko
Drinic - Univ. of California, Los Angeles, CA

25.4 A Framework for Object Oriented Hardware Specification, Verification, and Synthesis

Tommy Kuhn, Tobias Oppold, Markus Winterholer,
Wolfgang Rosenstiel - Univ. of Tuebingen,
Tuebingen, Germany
Marc Edwards - Cisco Systems,
Research Triangle Park, NC
Yaron Kashai - Verisity Design, Inc.,
Mountain View, CA



Wednesday
June 20

4:30
to
6:00

All speakers are
denoted in bold

S - denotes
short paper

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best paper

24

Session 26

rm: N111-N114

PANEL: WHEN WILL THE ANALOG DESIGN FLOW CATCH UP WITH DIGITAL METHODOLOGY?

CHAIR: *Georges Gielen* - Katholieke Univ., Leuven, Belgium

ORGANIZERS: *Mike Sottak, Mike Murray, Linda Kaye*

Despite the fact that more and more electronic design is comprised of analog and mixed signal content, the design flows and methodologies in this area are lagging behind the pace of innovation in digital design. For sure, analog designers are in shorter supply, but this only makes the need for improvements and efficiency that much greater. Only of late have we seen production-worthy attempts at functions such as analog synthesis and optimization reach the market. What is needed in today's analog design flow? What are the key technologies that are missing? How does the existing "food chain" need to work together to drive greater efficiencies? A distinguished panel of suppliers and users will analyze these issues and project future trends.

PANELISTS:

Mar Heishenson - Barcelona Design, Sunnyvale, CA

Ken Kundert - Cadence Design Systems, Inc., San Jose, CA

Phillipe Magarshack - ST Microelectronics, Crolles, France

Akira Matsuzawa - Matsushita, Osaka, Japan

Ronald Rohrer - Neolinear, Inc., Pittsburgh, PA

Ping Yang - TSMC, Richardson, TX

Session 27

rm: N109-N110

SPECIAL SESSION: CLOSING THE GAP BETWEEN ASIC AND CUSTOM: DESIGN EXAMPLES

CHAIR: *Bryan Ackland* - Agere Systems, Holmdel, NJ

ORGANIZER: *Kurt Keutzer*

A significant performance gap exists between integrated circuits designed in a custom methodology, and those designed in an ASIC (RTL synthesis) methodology. DAC hosted a session last year that focused on techniques to bridge this gap. This year's session looks at real circuit examples that have successfully done so.

27.1 Achieving 550Mhz in an ASIC Methodology

D.G. Chinnery, Bora Nikolic', Kurt Keutzer - *Univ. of California, Berkeley, CA*

27.2 A Semi-Custom Design Flow in High-Performance Microprocessor Design

Gregory A. Northrop, Pong-Fei Lu - *IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*

27.3 Reducing the Frequency Gap Between ASIC and Custom Designs: A Custom Perspective

Stephen E. Rich, Matthew J. Parker, Jim Schwartz - *Intel Corp., Hillsboro, OR*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 28

rm: N115-N117

ENERGY AND FLEXIBILITY DRIVEN SCHEDULING

CHAIR: Marco Di Natale - Univ. of Pisa, Pisa, Italy
ORGANIZERS: Donatella Sciuto, Luciano Lavagno

This session looks at several applications of static scheduling in the context of real time embedded systems. The first paper presents a voltage scheduling algorithm based on static timing analysis that controls the supply voltage to exploit all available slack. The second paper takes battery characterization into account to optimally schedule tasks in a real time embedded system. The third paper discusses how to implement new functionality on an already existing system such that running applications are not disturbed.

28.1 Low-Energy Intra-Task Voltage Scheduling Using Static Timing Analysis

Dongkun Shin, Jihong Kim - Seoul National Univ., Seoul, Korea
Seongsoo Lee - Ewha Woman's Univ., Seoul, Korea

28.2 Battery-Aware Static Scheduling for Distributed Real-Time Embedded Systems

Jiong Luo, Niraj K. Jha - Princeton Univ., Princeton, NJ

28.3 An Approach to Incremental Design of Distributed Embedded Systems

Paul Pop, Petru Eles, Traian Pop, Zebo Peng - Linköping Univ., Linköping, Sweden

Session 29

rm: N119-N120

REPRESENTATION AND OPTIMIZATION FOR DIGITAL ARITHMETIC CIRCUITS

CHAIR: Miodrag Potkonjak - Univ. of California, Los Angeles, CA

ORGANIZERS: Kazutoshi Wakabayashi, Rajesh K. Gupta

Optimization of arithmetic operations is crucial for many signal processing applications and more generally for datapath circuits in broader applications. The first paper in this session presents a novel signal representation for carry-save arithmetic optimizations across register boundaries. The second paper examines precision and signal clustering for improved data path designs. The last paper presents an approach for digital filter synthesis using the minimal signed digit representations.

29.1 Signal Representation Guided Synthesis Using Carry-Save Adders For Synchronous Data-Path Circuits

Zhan Yu - Univ. of California, Los Angeles, CA
Meng-Lin Yu - Lucent Technologies, Holmdel, NJ
Alan N. Willson Jr. - Univ. of California, Los Angeles, CA

29.2 Improved Merging of Datapath Operators Using Information Content and Required Precision Analysis

Anmol Mathur, Sanjeev Saluja - Cadence Design Systems, Inc., San Jose, CA

29.3 Digital Filter Synthesis Based on Minimal Signed Digit Representation

In Cheol Park, Hyeong Ju Kang - KAIST, Taejeon, Korea

Session 30

rm: N107-N108

TECHNIQUES FOR IP PROTECTION

CHAIR: Ian R. Mackintosh - Sonics Inc., Mountain View, CA
ORGANIZERS: Kenji Yoshida, Majid Sanafzadeh

The first three papers propose three new techniques for enabling watermarking of hardware IP. They introduce a technique for public authentication of hardware IP, an optimal watermarking technique with respect to credibility and a watermarking technique for partitioning. The last paper introduces a technique for measuring how many IC's are produced for a given licensed design.

30.1 Publicly Detectable Techniques for the Protection of Virtual Components

Gang Qu - Univ. of Maryland, College Park, MD

30.2 Watermarking of SAT Using Combinatorial Isolation Lemmas

Rupak Majumdar - Univ. of California, Berkeley, CA
Jennifer L. Wong - Univ. of California, Los Angeles, CA

30.3S Watermarking Graph Partitioning Solutions

Greg Wolfe, Jennifer L. Wong, Miodrag Potkonjak - Univ. of California, Los Angeles, CA

30.4S Hardware Metering

Farnaz Koushanfar - Univ. of California, Berkeley, CA
Gang Qu - Univ. of Maryland, College Park, MD



Thursday
June 21

8:30
to
10:00

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denoted in bold

S - denotes
short paper

β - denotes
best paper

Session 31

rm: N111-N114

SPECIAL SESSION: VISUALIZATION AND ANIMATION FOR VLSI DESIGN

CHAIR: Chandu Visweswariah - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY

ORGANIZERS: Chandu Visweswariah, Majid Sanafzadeh

This visually rich session will demonstrate the use of modern visualization and animation for dealing with large amounts of data to generate intuition about circuit behavior, large layouts or complex algorithms. These visualization methods are surprisingly accessible and easy to use. Eye-popping animation and visualization methods for understanding DSM interconnects, clock distribution networks, large VLSI layouts and various CAD-related algorithms will be shown.

31.1 Technical Visualizations in VLSI Design

Phillip Restle - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY

31.2 Using Texture Mapping with Mipmapping to Render a VLSI Layout

Jeffrey M. Solomon, **Mark A. Horowitz** - Stanford Univ., Stanford, CA

31.3 Web-Based Algorithm Animation

Marc Najork - Compaq Systems Research Ctr., Palo Alto, CA

Session 32

rm: N109-N110

APPLICATION-SPECIFIC CUSTOMIZATION FOR SYSTEMS-ON-A-CHIP

CHAIR: Kees Vissers - Trimedia Technologies Inc., Milpitas, CA

ORGANIZERS: Kurt Keutzer, Dirk Grunwald

This session examines a number of ways in which systems-on-a-chip can be adapted or customized for particular applications. The first paper looks at tailoring processor architectures for media applications. The second looks at exploring a family of multiprocessor architectures for communication problems. The third paper looks at customizations for power management.

32.1 Speeding Up Control-Dominated Applications through Microarchitectural Customizations in Embedded Processors

Peter Petrov, **Alex Orailoglu** - Univ. of California at San Diego, La Jolla, CA

32.2 Automatic Generation of Application-Specific Architectures for Heterogeneous Multiprocessor System-on-Chip

Damien Lyonnard, **Sungjoo Yoo**, **Amer Baghdadi**, **Ahmed A. Jerraya** - TIMA Lab., Grenoble, France

32.3 Dynamic Voltage Scaling for Portable Systems

Tajana Simunic - Stanford Univ., Stanford, CA

Session 33

rm: N115-N117

SATISFIABILITY SOLVERS AND TECHNIQUES

CHAIR: *Karem Sakallah - Univ. of Michigan, Ann Arbor, MI*
ORGANIZERS: *Andrew B. Kahng, Kurt Keutzer, Limor Fix*
Boolean satisfiability techniques have been used successfully in a variety of EDA applications such as formal verification, testing and timing analysis. This session presents new and advanced satisfiability solvers and techniques that dramatically advance the performance of Boolean Satisfiability engines, and extend their scope to incremental formulations.

33.1 Engineering a (Super?) Efficient SAT Solver

Matthew W. Moskewicz - Univ. of California, Berkeley, CA
Conor F. Madigan - Massachusetts Institute of Tech., Boston, MA
Ying Zhao, Lintao Zhang, Sharad Malik - Princeton Univ., Princeton, NJ

33.2 Dynamic Detection and Removal of Inactive Clauses in SAT with Application in Image Computation

Aarti Gupta - NEC USA, Princeton, NJ
Anubhav Gupta - Carnegie Mellon Univ., Pittsburgh, PA
Zijiang Yang, Pranav N. Ashar - NEC USA, Princeton, NJ

33.3S SATIRE: A New Incremental Satisfiability Engine

Jesse P. Whittlemore - Univ. of Michigan, Ann Arbor, MI

Joonyoung Kim - Intel Corp., Hillsboro, OR
Karem A. Sakallah - Univ. of Michigan, Ann Arbor, MI

33.4S A Framework for Low Complexity Static Learning

Emil I. Gizdarski, Hideo Fujiwara - Nara Institute of Science and Tech., Ikoma, Japan

Session 34

rm: N119-N120

POWER AND INTERCONNECT ANALYSIS

CHAIR: *L. Miguel Silveira - INESC/IST, Lisboa, Portugal*
ORGANIZERS: *Joel Phillips, Mustafa Celik*

This session features papers in power issues — energy dissipation of interconnect, power network analysis and optimization. A final contribution presents a method for high-frequency inductance calculations.

34.1 Fast Power/Ground Network Optimization Based on Equivalent Circuit Modeling

X.-D. Sheldon Tan - Altera Corp., San Jose, CA
C.-J. Richard Shi - Univ. of Washington, Seattle, WA

34.2S An Interconnect Energy Model Considering Coupling Effects

Taku Uchino, Jason Cong - Univ. of California, Los Angeles, CA

34.3S Efficient Large-Scale Power Grid Analysis Based on Preconditioned Krylov-Subspace Iterative Methods

Tsung-Hao Chen, Charlie Chung-Ping Chen - Univ. of Wisconsin, Madison, WI

34.4S Using Conduction Modes Basis Functions for Efficient Electromagnetic Analysis of On-Chip and Off-Chip Interconnect

Luca Daniel, Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA
Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

34.5S Analysis of Non-Uniform Temperature-Dependent Interconnect Performance in High Performance ICs

Amir H. Ajami - Univ. of Southern California, Los Angeles, CA
Kaustav Banerjee - Stanford Univ., Stanford, CA
Massoud Pedram - Univ. of Southern California, Los Angeles, CA
Lukas P.P.P. van Ginneken - Magma Design Inc., Cupertino, CA

Session 35

rm: N107-N108

DOMAIN SPECIFIC DESIGN METHODOLOGIES

CHAIR: *Yosinori Watanabe - Cadence Berkeley Labs., Berkeley, CA*

ORGANIZERS: *Anand Raghunathan, Shin-ichi Minato*

In this session, we explore design methodologies that focus on specific application domains. The paper attacks the following three domain instances: direct digital frequency synthesizers for communication systems, symmetric block ciphers for cryptographic analysis, Viterbi decoders and IIR filters in DSPs. These case studies will hint at new methodologies for designing real-life applications.

35.1 VHDL Based Design and Design Methodology for Reusable High Performance Direct Digital Frequency Synthesis

Ireneusz Janiszewski, Bernhard Hoppe, Hermann Meuth - FH Darmstadt, Darmstadt, Germany

35.2 Concurrent Error Detection Schemes for Side-Channel Fault-Analysis of 128-bit Symmetric Block Ciphers

Ramesh Kari, Kaijie Wu, Piyush Mishra - Polytechnic Univ., Brooklyn, NY
Yongkook Kim - IBM Corp., Poughkeepsie, NY

35.3 MetaCores: Design and Optimization Techniques

Seapahn Meguerdichian, Farinaz Koushanfar - Univ. of California, Los Angeles, CA
Advait Mogre, Dusan Petranovic - LSI Logic Corp., Milpitas, CA
Miodrag Potkonjak - Univ. of California, Los Angeles, CA



Thursday
June 21

10:30
to
12:00

All speakers are
denoted in bold

S - denotes
short paper

β - denotes
best paper

28

Session 36

rm: N111-N114

PANEL: DEBATE: WHO HAS NANOMETER DESIGN UNDER CONTROL?

CHAIR: Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA
ORGANIZER: Bing Sheu

As fabrication technology moves to 100 nm and below, profound nanometer effects become critical in developing silicon chips with hundreds of millions of transistors. Both EDA suppliers and system houses have been re-tooling, and new methodologies have been emerging. Will these efforts meet the challenges of nanometer silicon such as performance closure, power, reliability, manufacturability, and cost? Which aspects of nanometer design are, or are not, under control? This session will consist of a debate between two teams of distinguished representatives from EDA suppliers and system design houses. Which side has the right answers and roadmap? You and a panel of judges will decide!

PANELISTS:

Shekhar Borkar - Intel Corp., Hillsboro, OR
Ed Cheng - Synopsys, Inc., Mountain View, CA
John Cohn - IBM Corp., Essex Junction, VT
Nancy Nettleton - Sun Microsystems, Mountain View, CA
Lou Scheffer - Cadence Design Systems, Inc., San Jose, CA
Sang Wang - Nassda Corp., Santa Clara, CA

Session 37

rm: N109-N110

ANALYSIS AND IMPLEMENTATION FOR EMBEDDED SYSTEMS

CHAIR: Grant Martin - Cadence Design Systems, Inc., San Jose, CA
ORGANIZERS: Dirk Grunwald, Kurt Keutzer, Luciano Lavagno

This set of papers describes system level design tools and design flows for system design, performance trade offs and power estimation. The first paper uses simulink for rapid design of data-dominated applications. The remaining papers provide power models using automatic formalisms and the other using a combination of design captive and application characteristics.

37.1 A Hardware/Software Co-Design Flow and IP Library Based on Simulink

Leonardo Reyneri, Francesco Cucinotta, **Alessandro Sera** -
Politecnico di Torino, Turin, Italy
Luciano Lavagno - *Univ. di Udine, Udine, Italy*

37.2 System-Level Power/Performance Analysis for Embedded Systems Design

Amit Nandi, Radu Marculescu - *Carnegie Mellon Univ.,
Pittsburgh, PA*

37.3 High-Level Software Energy Macro-Modeling

Tat K. Tan - *Princeton Univ., Princeton, NJ*
Anand Raghunathan, Ganesh Lakshminarayana - *NEC USA,
Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 38

rm: N115-N117

INDUSTRIAL CASE STUDIES IN VERIFICATION

CHAIR: Carl Pixley - Motorola, Inc., Austin, TX
ORGANIZERS: Anand Raghunathan, Carl Pixley

Verification is well-known to be one of the most expensive, delaying and critical aspects of the design process. We present three industrial case studies that illustrate novel approaches to integrating functional verification techniques: simulation, emulation and formal verification.

38.1 Model Checking of S3C2400X Industrial Embedded SoC Product

Hoon Choi, Byeongwee Yun, Yuntae Lee,
Hyunglae Roh - Samsung Electronics, Yongin, Korea

38.2 Semi-Formal Test Generation with Genevieve

Julia Dushina, Mike Benjamin -
ST Microelectronics, Bristol, UK
Daniel Geist - IBM Corp., Haifa, Israel

38.3 A Transaction-Based Unified Simulation/Emulation Architecture for Functional Verification

Murali Kudlugi - IKOS Systems, Inc., Waltham, MA
Soha Hassoun - Tufts Univ., Medford, MA
Charles Selvidge - IKOS Systems, Inc., Waltham, MA
Duaine Piyor - IKOS Systems, Inc., Cupertino, CA

Session 39

rm: N119-N120

INTEGRATED HIGH-LEVEL SYNTHESIS BASED SOLUTIONS

CHAIR: Kazutoshi Wakabayashi - NEC Corp.,
Kawasaki, Japan

ORGANIZERS: Kazutoshi Wakabayashi, Rajesh K. Gupta

The focus of this session is on design flows that seek to integrate high-level synthesis into physical design. The first paper presents integration of HLS with power-net design targeted for mixed signal ICs. The second paper considers HLS with placement targeted for reconfigurable computing architectures. The last paper explores design exploration using multiple HLS tools.

39.1 Integrated High-Level Synthesis and Power-Net Routing for Digital Design under Switching Noise Constraints

Alex Doboli - State Univ. of New York,
Stony Brook, NY

Ranga Vemuri - Univ. of Cincinnati, Cincinnati, OH

39.2 Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures

Kia Bazargan - Univ. of Minnesota, Minneapolis, MN
Seda Ogrenic, Majid Sarrafzadeh - Univ. of
California, Los Angeles, CA

39.3 Statistical Design Space Exploration for Application-Specific Unit Synthesis

Davide Bruni - Univ. di Bologna, Bologna, Italy
Alessandro Bogliolo - Univ. di Ferrara, Ferrara, Italy
Luca Benini - Univ. di Bologna, Bologna, Italy

Session 40

rm: N107-N108

TIMING VERIFICATION AND SIMULATION

CHAIR: Ashok Vittal - Synopsys, Inc., Mountain View, CA
ORGANIZER: Narendra Shenoy

This session deals with various aspects of timing issues including analysis, optimization, characterization and modeling for simulation that arise in EDA. Paper one describes techniques to support efficient verification with complex timing variations. Optimizing for crosstalk effects is the subject of paper two. Paper three is relevant in the context of sub-circuit characterization. Paper four deals with scheduling and synchronization for multiple clock domains.

40.1 Static Scheduling of Multiple Asynchronous Domains for Functional Verification

Murali Kudlugi, Charles Selvidge - IKOS Systems,
Inc., Waltham, MA
Russell G. Tessier - Univ. of Massachusetts,
Amherst, MA

40.2S Functional Correlation Analysis in Crosstalk Induced Critical Paths Identification

Tong Xiao - Sun Microsystems, Inc., Palo Alto, CA
Malgorzata Marek-Sadowska - Univ. of California,
Santa Barbara, CA

40.3S An Advanced Timing Characterization Method Using Mode Dependency

Hakan Yalcin, Robert Palermo, Mohammad S.
Mortazavi - Cadence Design Systems, Inc.,
San Jose, CA

Cyrus S. Bamji - Canesta Inc., Santa Clara, CA
Karem A. Sakallah, John P. Hayes - Univ. of
Michigan, Ann Arbor, MI

40.4 Fast Statistical Timing Analysis By Probabilistic Event Propagation

Jing-Jia Liou, Kwang-Ting Cheng - Univ. of
California, Santa Barbara, CA
Sandip Kundu - Intel Corp., Austin, TX
Angela Krstic - Univ. of California, Santa
Barbara, CA



Thursday
June 21

2:00
to
4:00

All speakers are
denoted in bold

S - denotes
short paper

β - denotes
best paper

30

Session 41

rm: N111-N114

SPECIAL SESSION: ON-CHIP COMMUNICATION ARCHITECTURES

CHAIR: Anand Raghunathan - NEC USA C&C Research Lab., Princeton, NJ
ORGANIZERS: Anand Raghunathan, Sharad Malik

Designing a high quality communication architecture is increasingly becoming critical to meeting performance, power, and turn around time constraints in the design of System-on-Chips. This special session consists of invited presentations from designers of on-chip communication architectures used today, as well as researchers involved in developing architectures and design methodologies of the future. The first presentation will highlight the role played by on-chip communication architectures in system design, describe the challenges involved, and present a communication-based design paradigm. The second presentation will describe how micro-network based architectures can be used to implement communication between SoC components. The third presentation will provide a design example from the domain of high-performance network processors, focusing on the challenges involved in on-chip communication, and how they are addressed. The final presentation will examine technology trends and their implications on on-chip communication architecture design, arguing the case for the use of packet-switched on-chip networks.

41.1 Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design

Jan Rabaey, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Sharad Malik - *Princeton Univ., Princeton, NJ*
Kurt Keutzer - *Univ. of California, Berkeley, CA*

41.2 MicroNetwork-Based Integration for SOCs

Drew Wingard - *Sonics, Inc., Mountain View, CA*

41.3 On-Chip Communication Architecture for OC-768 Network Processors

Faraydon Karim, Anh Nguyen - *ST Microelectronics, San Diego, CA*
Sujit Dey, Ramesh Rao - *Univ. of California at San Diego, La Jolla, CA*

41.4 Route Packets, Not Wires: On-Chip Interconnection Networks

William Dally - *Stanford Univ., Stanford, CA*

Session 42

rm: N109-N110

COMPILER AND ARCHITECTURE INTERACTIONS

CHAIR: Stephen Neuendorffer - *Univ. of California, Berkeley, CA*
ORGANIZERS: Donatella Sciuto, Marco Di Natale

The efficient use and simulation of architecture components requires a fine tuning of the compiler algorithms or even a tight integration between components and compiler design. This session contains four papers spanning from compiler optimization techniques for reducing data transfers in clustered VLIW architectures to compiler-controlled scratch-pad memory management, to fast simulation of fixed point systems through code transformation.

42.1 Dynamic Management of Scratch-Pad Memory Space

Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
J. Ramanujam - *Louisiana State Univ., Baton Rouge, LA*
Mary Jane Irwin, Vijaykrishnan Narayanan, Ismail Kadayif, Amisha Parikh - *Penn State Univ., University Park, PA*

42.2 Clustered VLIW Architectures with Predicated Switching

Margarida F. Jacome, Gustavo A. de Veciana, Satish Pillai - *Univ. of Texas, Austin, TX*

42.3 High-Quality Operation Binding for Clustered VLIW Datapaths

Viktor S. Lapinskii, Margarida F. Jacome, Gustavo A. de Veciana - *Univ. of Texas, Austin, TX*

42.4 Fast Bit-True Simulation

Holger Keding, Martin Coors, Olaf Luethje, Heinrich Meyr - *Integrated Signal Processing Systems, Aachen, Germany*

Session 43

rm: N115-N117

TIMING WITH CROSSTALK

CHAIR: Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

ORGANIZERS: Jaijeet Roychowdhury, Mustafa Celik

This session deals with the impact of crosstalk on timing. The first paper uses a theoretical approach to analyze some practical issues such as convergence. The second paper introduces a new driver model for accurate coupled noise modeling and then discusses worst case alignment. The third paper uses functional information to eliminate false coupling interactions to avoid pessimistic delay calculation. The last paper proposes a post-layout optimization technique to reduce coupling induced delay.

43.1 Timing Analysis with Crosstalk as Fixpoints on Complete Lattice

Hai Zhou, Narendra Shenoy, William Nicholls - Synopsys, Inc., Mountain View, CA

43.2 Driver Modeling and Alignment for Worst-Case Delay Noise

Supamas Siichotiyakul, David Blaauw, Chanhee Oh - Motorola, Inc., Austin, TX
Rafi Levy - Motorola, Inc., Herzelia, Israel
Vladimir Zolotov, Jingyan Zuo - Motorola, Inc., Austin, TX

43.3 False Coupling Interactions in Static Timing Analysis

Ravishankar Anunachalam, Ronald D. Blanton, Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

43.4 Coupling Delay Optimization by Temporal Decorrelation using Dual Threshold Voltage Technique

Kiwook Kim, Seong Ook Jung - Univ. of Illinois, Urbana, IL
Prashant Saxena - Intel Corp., Portland, OR
Chaung Laung Liu - National Tsing-Hua Univ., Hsinchu, Taiwan, ROC
Sung Mo Kang - Univ. of Illinois, Urbana, IL

Session 44

rm: N119-N120

LOW POWER DESIGN: SYSTEMS TO INTERCONNECT

CHAIR: Vivek Tiwari - Intel Corp., Santa Clara, CA

ORGANIZERS: Ingrid Verbauwhede, Tadahiro Kuroda

Low Power design needs to be addressed at all levels. At the system level, the first paper presents a generalized approach to the concept of partitioning the input space and applying specific optimizations to the partitions for overall energy reduction. The issue of energy consumption in DSM interconnects has gained attention recently. The next three papers present an introduction and different approaches to the problem. The final paper describes the circuit design of an adiabatic multiplier.

44.1 Input Space Adaptive Design: A High-Level Methodology for Energy and Performance Optimization

Weidong Wang - Princeton Univ., Princeton, NJ
Ganesh Lakshminarayana, Anand Raghunathan - NEC USA, Princeton, NJ

Niraj K. Jha - Princeton Univ., Princeton, NJ

44.2 A2BC: Adaptive Address Bus Coding for Low Power Deep Sub-Micron Designs

Joerg Henkel - NEC USA, Princeton, NJ

44.3S Coupling-Driven Bus Design for Low-Power Application-Specific Systems

Youngsoo Shin, Takayasu Sakurai - Univ. of Tokyo, Tokyo, Japan

44.4S Modeling and Minimization of Interconnect Energy Dissipation in Nanometer Technologies

Clark N. Taylor, Sujit Dey, Yi Zhao - Univ. of California at San Diego, La Jolla, CA

44.5 Student Design Contest: A True Single-Phase 8-bit Adiabatic Multiplier

Suhwan Kim - IBM Corp., Yorktown Heights, NY
Conrad H. Ziesler, Marios C. Papaefthymiou - Univ. of Michigan, Ann Arbor, MI

Session 45

rm: N107-N108

FLOORPLANNING REPRESENTATIONS AND PLACEMENT ALGORITHMS

CHAIR: Ralph H.J.M. Otten - Delft Univ. of Technology, Delft, The Netherlands

ORGANIZERS: Louis Scheffer, Patrick Groeneveld

The first two papers offer improved representations for floorplanning, offering faster incremental updates and capable of handling a wider variety of block shapes and constraints. The next two papers are improvements of partitioning based placement, providing better quality of results in wire length and timing. The final paper takes a novel approach, using system level power considerations to drive partitioning and placement.

45.1 TCG: A Transitive Closure Graph-Based Representation for Non-Slicing Floorplans

Jai-Ming Lin, Yao-Wen Chang - National Chiao Tung Univ., Hsinchu, Taiwan, ROC

45.2 Floor planning with Abutment Constraints and L-Shaped/T-Shaped Blocks Based on Corner Block List

Yuchun Ma, Xianlong Hong, Sheqin Dong, Yici Cai - National Tsing-Hua Univ., Beijing, China

Chung-Kuan Cheng - Univ. of California at San Diego, La Jolla, CA

Jun Gu - Science and Tech. Univ. of Hong Kong, Hong Kong, China

45.3S Improved Cut Sequences for Partitioning Based Placement

Patrick H. Madden, Mehmet C. Yildiz - State Univ. of New York, Binghamton, NY

45.4S Timing Driven Placement using Physical Net Constraints

Bill M. Halpin - Intel Corp., Santa Clara, CA/Syracuse Univ., Syracuse, NY

C. Y. Roger Chen - Syracuse Univ., Syracuse, NY

Naresh K. Sehgal - Intel Corp., Santa Clara, CA

45.5 From Architecture to Layout: Partitioned Memory Synthesis for Embedded Systems-on-Chip

Luca Benini - Univ. di Bologna, Bologna, Italy

Luca Macchiarulo, Alberto Macii, Enrico Macii,

Massimo Poncino - Politecnico di Torino, Torino, Italy



Thursday
June 21

4:30
to
6:00

All speakers are
denoted in bold

S - denotes
short paper

β - denotes
best paper

32

Session 46

rm: N111-N114

PANEL: WHAT DRIVES EDA INNOVATION?

CHAIR: Steve Schulz - Texas Instruments, Dallas, TX
ORGANIZER: Georgia Maiszalek

If EDA technology innovation drives return on investment, what drives innovation? Is it tied to the semiconductor retooling cycle? To productivity requirements? To Moore's Law? Or is there something more fundamental that we are missing? What driving forces could result in a \$30 billion EDA industry, and what role will innovation play? Will the industry provide the needed breakthroughs for their customers, or seek instead the lowest common denominator user? Will designers "roll their own" tools or seek common solutions? How does EDA innovation track with the semiconductor business cycle? Does a slowdown accelerate or depress creation of new tools and new designs? Panelists will discuss the forces at work in the EDA industry of tomorrow.

PANELISTS:

John Daminger - IBM Corp., Yorktown Heights, NY
Greg Hinckley - Mentor Graphics Corp., Wilsonville, OR
George Janac - InTimeSoftware, Inc., Cupertino, CA
Handel Jones - International Business Strategies, Los Gatos, CA
Greg Spirakis - Intel Corp., Santa Clara, CA
Karen Vahtra - Magma Design Automation, Inc., Cupertino, CA

Session 47

rm: N109-N110

SIGNAL INTEGRITY: AVOIDANCE AND TEST TECHNIQUES

CHAIR: Anirudh Devgan - IBM Corp., Austin, TX
ORGANIZERS: Chandu Visweswaniah, Kenji Yoshida

Inductive effects in interconnect are a major source of headaches for state-of-the-art digital designs. Inductive effects cause nasty timing and noise problems and threaten to be show-stoppers. This session features three innovative techniques to solve, avoid or test for these problems.

47.1 Built-In Self-Test for Signal Integrity

Mehrdad Nourani, Amir Attarha - Univ. of Texas at Dallas, Richardson, TX

β 47.2 Analysis of On-Chip Inductance Effects using a Novel Performance Optimization Methodology for Distributed RLC Interconnects

Kaustav Banerjee - Stanford Univ., Stanford, CA
Amit Mehrotra - Univ. of Illinois, Urbana, IL

47.3 Modeling and Analysis of Differential Signaling for Minimizing Inductive Cross-Talk

Yehia M. Massoud, Jamil Kawa, Don MacMillen - Synopsys, Inc., Mountain View, CA
Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 48

rm: N115-N117

NOVEL APPROACHES TO MICROPROCESSOR DESIGN AND VERIFICATION

CHAIR: Derek Beatty - Motorola, Inc., Austin, TX

ORGANIZERS: Carl Pixley, Shin-ichi Minato

This session covers novel approaches to the correct design and verification of complex microprocessors, including automatic design of interlock and forwarding logic, generation of test programs to exercise complex corner cases, and verification techniques for the error logic.

48.1 Automated Pipeline Design

Daniel Kroening, Wolfgang Paul - Univ. of Saarland, Saarbruecken, Germany

48.2 A New Verification Methodology for Complex Pipeline Behavior

Kazuyoshi Kohno, Nobu Matsumoto - Toshiba Corp., Kawasaki, Japan

48.3 Pre-Silicon Verification of the Alpha 21364 Microprocessor Error Handling System

Richard Lee, Benjamin Tsien - Compaq Computer Corp., Palo Alto, CA

Session 49

rm: N119-N120

SCHEDULING TECHNIQUES FOR POWER MANAGEMENT

CHAIR: Donatella Sciuto - Politecnico di Milano, Milano, Italy

ORGANIZERS: Diederik Verkest, Luciano Lavagno

Power constraints become increasingly important in embedded systems. This session presents new scheduling techniques for power management under different circumstances. The first paper presents a technique to determine voltage settings for a variable voltage processor. The second paper introduces a formal model of distributed multimedia systems that enables determining an optimal power management policy. The third paper looks at power aware scheduling in the context of mission critical systems.

49.1 Energy Efficient Fixed-Priority Scheduling for Real-Time Systems on Variable Voltage Processors

Gang Quan, Xiaobo (Sharon) Hu - Univ. of Notre Dame, Notre Dame, IN

49.2 Dynamic Power Management in a Mobile Multimedia System with Guaranteed Quality-of-Service

Qing Wu, Massoud Pedram, Qinru Qiu - Univ. of Southern California, Los Angeles, CA

49.3 Power-Aware Scheduling under Timing Constraint for Mission-Critical Embedded Systems

Jinfeng Liu, Pai H. Chou, Nader Bagherzadeh - Univ. of California, Irvine, CA

Session 50

rm: N107-N108

NOVEL DEVICES AND YIELD OPTIMIZATION

CHAIR: Chandu Visweswariah - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY

ORGANIZERS: Chandu Visweswariah, Ralph H.J.M. Otten

How soon will novel devices revolutionize integrated circuits? What can we do about falling yields due to mismatch and intra-chip variations? This session takes a shot at answering these questions. It begins with description of novel 3-dimensional SOI devices and then a novel MEMS accelerometer for mouse applications. Finally, yield optimization due to mismatch problems is addressed.

50.1 Exploring SOI Device Structures and Interconnect Architectures for 3-Dimensional Integration

Rongtian Zhang, Kaushik Roy, Cheng Kok Koh, David B. Janes - Purdue Univ., West Lafayette, IN

50.2 Student Design Contest: Two-Dimensional Position Detection System with MEMS Accelerometer for MOUSE Applications

Seungbae Lee, Gi-Joon Nam, Junseok Chae, Hanseup Kim, Alan J. Drake - Univ. of Michigan, Ann Arbor, MI

50.3 Mismatch Analysis and Direct Yield Optimization by Spec-Wise Linearization and Feasibility-Guided Search

Frank Schenkel, Michael Pronath - Tech. Univ. of Munich, Munich, Germany
Stephan Zizala, Robert Schwencker, Helmut Graeb - Infineon Technologies, Munich, Germany
Kurt Antreich - Tech. Univ. of Munich, Munich, Germany



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Tutorial 1

Friday, June 22

Tutorials will be held at the Las Vegas Convention Center.

8:00 AM - 1:00 PM Tutorial Registration Open

9:00 AM - 5:00 PM Tutorials

8:00 AM - Continental Breakfast - Room N246, N250

12:00 Noon - Lunch - Room N246, N250

DESIGN-FOR-TEST TECHNIQUES FOR SoC DESIGNS

rm: N115 - N117

ORGANIZER: *Janusz Rajski* - Mentor Graphics Corp., Willsonville, OR
PRESENTERS: *Janusz Rajski* - Mentor Graphics Corp., Willsonville, OR
Alfred Crouch - Motorola, Inc., Austin, TX
Geir Eide - Mentor Graphics Corp., Wilsonville, OR

Audience: Designers of complex systems-on-a-chip and ASICs, IP core providers, SoC integrators, system architects, and design managers interested in learning about state-of-the-art DFT technology, practices and automation tools.

Description: Complex SoC designs contain millions of gates of logic and, in some cases, hundreds of embedded memories. In a complex SoC design process, Design-for-Test is one of the crucial components that determine the time to market, product quality, and its manufacturing cost. This tutorial aims to jump start the designer to new levels of practical test expertise by presenting DFT methodologies, solutions, and technological advancements for addressing today's toughest DFT issues. The tutorial briefly introduces basic DFT concepts and techniques, and focuses on practical issues such as: IP core design guidelines that enable test reuse, DFT for complex SoC designs, embedded memory test, at-speed test, and DFT integration into the design flow. More specifically the tutorial presents in detail structural Design-for-Test methodologies based on scan, i.e. scan cell design, scan operation, scan chain optimization, multiple clock domains, test logic, test points, basic concepts of Logic BIST, and boundary scan. Automatic test

pattern generation (ATPG) creates high quality, compact test patterns in a fully automated manner. The highlights of the section addressing ATPG include: design rules checking, random and deterministic test pattern generation, pattern compression techniques, test pattern verification, combinational and sequential pattern types, and at-speed test.

A special section of the tutorial is devoted to testing of embedded memories. It reviews: memory types, fault models, test algorithms, and test methods (Memory BIST and Vector translation).

The final section focuses on core test and SoC test integration. This chapter covers DFT in the design cycle, scan insertion flow, physical aspects of SoC DFT, test wrappers for IP cores, design guidelines and recommendations for test reuse, hierarchical test pattern generation, test access mechanisms, test scheduling, SoC test integration and verification. Important concepts and methodologies are illustrated by practical applications and case studies.



Tutorial 2

Friday, June 22

INTERACTIVE TUTORIAL ON FUNDAMENTALS OF SIGNAL INTEGRITY FOR HIGH-SPEED/HIGH-DENSITY DESIGN

rm: N109 - N110

ORGANIZERS: *Andreas Cangellaris* - Univ. of Illinois, Urbana, IL
José Schutt-Ainé - Univ. of Illinois, Urbana, IL
PRESENTERS: *Andreas Cangellaris* - Univ. of Illinois, Urbana, IL
Alina Deutsch - IBM Corp., Yorktown Heights, NY
Umberto Ravaioli - Univ. of Illinois, Urbana, IL
José Schutt-Ainé - Univ. of Illinois, Urbana, IL

Audience: PCB and chip designers who want to gain familiarity with signal integrity issues at high-speeds and who want to develop a more practical approach for designing high-speed modules and high-density chips. Knowledge of basic transmission line theory will be helpful.

Description: With the advent of fast processors and high frequency communication networks, the demand for more accurate computer-aided design (CAD) tools has increased dramatically. Faster signals and higher packing density have exacerbated the noise issues in state-of-the-art IC and package designs. This course will offer an in-depth understanding of the fundamental mechanisms that govern broadband signal transmission in interconnect structures at the different levels of integration. Signal transmission attributes and proper interconnect modeling on-chip and off-chip will be explained and demonstrated through the use of JAVA applets that will be made available to the course participants.

Particular emphasis will be placed on the present-day on-chip wiring design practices and the unique properties of on-chip lossy transmission lines. The deficiencies of RC-circuit-representation-based designs and tools will be highlighted through relevant examples. The shortcomings of some of the RLC-based available tools will also be explained. It will be shown that frequency-dependent resistive and inductive effects (R(f)L(f)C-circuit-representation) are especially important for crosstalk, common-mode noise, and clock skew. Guidelines will be given for design, technology scaling, device sizes used, noise containment, length tradeoffs, clock distribution, operating temperature, and bandwidth improvement. The need for multi-variable performance-driven routers based on worst-case delay, propagated rise-time, and crosstalk will be explained in order to make adequate use of available technologies.



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Tutorial 3

Friday, June 22

CAD TOOLS FOR MIXED-SIGNAL AND RF ICs

rm: N111 - N112

ORGANIZER: *Georges Gielen* - Katholieke Univ., Leuven, Belgium
PRESENTERS: *Georges Gielen* - Katholieke Univ., Leuven, Belgium
Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
Jaijeet Roychowdhury - CeLight, Inc., Springfield, NJ
Francois Clement - Simplex Solutions Inc., Grenoble, France

Audience: Practicing analog, RF and mixed-signal designers who want to learn about the new techniques and methodologies that could boost their design quality and productivity. CAD professionals responsible for implementing or maintaining analog, RF or mixed-signal tools or flows. Anyone with interests in practical RF or mixed-signal ICs.

Description: The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the technology. In addition, with the evolution towards ultra deep submicron CMOS technologies, the design of complex systems on a chip (SoC) will emerge which are increasingly mixed-signal designs. The desire to do hand-crafted, one-transistor-at-a-time analog design is increasingly at odds with the current time-to-market constraints and hence the need for more analog design productivity, practical circuit and layout synthesis, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial will present the recent progress and current state of the art in design tools and methodologies for complex mixed-signal designs as well as for RF IC design. Different aspects will be covered by the different presenters, ranging from techniques and methodologies for analog synthesis both at architectural, circuit and layout level, as well as the recent progress in simulation and modeling for RF designs, as well as methods to analyze substrate noise couplings in mixed-signal ICs. The techniques will be addressed from a designer point of view, so that the attendees can assess how the techniques could be integrated to improve their current design practice.

The tutorial is divided in 4 parts. The first part will describe tools for designing analog building blocks. The second part will present tools for high-level design and simulation of mixed-signal systems. The third part will describe modeling and simulation techniques for RF circuits. The final part will describe methods for the analysis of substrate noise coupling problems in mixed-signal ICs.



DESIGN-MANUFACTURING INTERFACE FOR UDSM ERA: DESIGNER AND CAD TOOL DEVELOPER PERSPECTIVES

ORGANIZER: *Andrzej J. Strojwas* - Carnegie Mellon Univ., Pittsburgh, PA
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rm: N113 - N114

Audience: The subtitle of this tutorial is: "What every designer and CAD tool developer should know about the implications of the Ultra Deep Submicron reality on the gigascale product design, verification and manufacturability". It is intended for all system and IC designers, CAD tool developers and university researchers. No IC technology/manufacturing background is required as a prerequisite.

Description: In this age of multi-billion dollar IC fablines and increased time-to-market pressures, achieving profitable production in the shortest possible time becomes an absolutely necessary condition for success. Increasing the initial yield and the rate of the yield ramp has the biggest impact on the product profitability. This task is especially challenging given the disaggregation of semiconductor industry, i.e., emergence of fabless companies and increasing role of foundries in manufacturing. This complex interface between "mother nature", represented by manufacturing process, and the design domain, focused more and more on higher levels of design abstraction, cannot be covered by a simple set of layout design rules and SPICE files to represent all essential relationships. The purpose of this tutorial is to depict a reality of the design-manufacturing interface in a manner useful to IC designers and CAD tool developers.

We will start by presenting an overview of trends in semiconductor industry focusing on the accelerated roadmap which leads to further miniaturization and the increasing role of manufacturing fluctuations. In the big picture, the most important link between design and manufacturing is quantified via manufacturing yield, which must be maximized during IC fabrication but is strongly determined by the design decisions made at all design abstraction levels. Therefore, manufacturing-aware design flow must rely on a spectrum of yield models. We will review in detail such models in the first part of the tutorial.

However, yield modeling cannot be useful if the models are not tuned to process reality and therefore cannot capture IC design sensitivity to process imperfections. To address this issue, the next part of our tutorial will be devoted to process/design characterization techniques/strategies via a comprehensive set of characterization vehicles to identify the key yield loss reasons (systematic, parametric, random defects). We will then discuss abstraction of manufacturability/reliability design rules including sub-wavelength lithography (OPC, PSM) and realistic worst-case SPICE files. These DFM interface capabilities will re-define the design flow and will pose new requirements on the EDA tools. They will enable much more predictive design synthesis and much more realistic verification of the system before its manufacturing. The bulk of our tutorial will propose such a design flow utilizing this DFM interface. We will focus on the following key tasks: technology choice (including monolithic vs. MCM, forecasting of performance, yield ramp-up and cost), high level design decisions using technology abstraction (choice of IP cores, IP migration vs. re-synthesis, etc.), estimation/optimization of timing, signal integrity and power, taking into account manufacturing fluctuations, circuit design optimization for SoC - including mixed-signal components (design centering, timing optimization) and layout optimization (including pre-tapeout optimization and post-tapeout transformations such as model-based OPC).

We will conclude the tutorial by discussing the technical and organizational challenges that must be overcome to successfully implement this new design-manufacturing interface.



The 38th Design Automation Conference • June 18 - 22, 2001 • Las Vegas, NV

Tutorial 5

Friday, June 22

LOW POWER TOOLS AND METHODOLOGIES FOR THE ASIC INDUSTRY

rm: N119 - N120

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PRESENTERS: *Enrico Macii* - Politecnico di Torino, Torino, Italy
Jeny Frankil - Sequence Design Inc., Acton, MA
Renu Mehra - Synopsys, Inc., Mountain View, CA
Mike Lee - Incentia Design Systems, Inc., Santa Clara, CA
Roberto Zafalon - ST Microelectronics, Agrate Brianza, Italy

Audience: This tutorial is primarily intended for ASIC designers, planners and project managers who are looking for practical solutions for reducing power in their designs. The focus is on power-aware design flows/methodology based on CAD solutions that are available today. It is hoped that attendees will come away with an understanding of the issues, tradeoffs and benefits of low power tools and will be able to effectively apply this knowledge to their designs and design flows.

Description: Power has been trending higher on the list of design constraints and today it is at or near the top across all computing platforms - whether this be laptops, cell-phones, hand-held PDAs, rack-mounted web-servers, routers, or big-iron servers in a backroom. Power is no longer a concern for only the thermally constrained high-performance (high-power) systems and energy-constrained low-power hand-held/portable systems. An ever-growing number of ASIC designs in all domains (chipsets, graphics, networking, media-processing, communication, etc.) are now faced with tight power budgets. Designers, many of whom are confronting this challenge for the first time, are looking for solutions they can use. There is large body of literature now on low power techniques, algorithms and tools, but this is not directly applicable to designers who do not have the luxury of creating or optimizing their own libraries, incorporating the latest modeling advance into their power estimation tools, or extending their synthesis tools with

the latest algorithms. For these designers, what works are: a) best-known methods for optimizing their logic - RTL description, either manually or through automation; b) ready-made estimation tools than can provide early feedback during the RTL-phase; c) estimation tools that provide feedback during or after synthesis and that can be used to direct the synthesis tools; and d) optimization algorithms built into the synthesis solutions.

The tutorial is structured to provide information on the state of the art in all these domains. It will start by motivating the need of industrial design frameworks (i.e., combination of design techniques and CAD tools) that explicitly address power minimization. A possible design flow for low-power ASICs will be proposed next. A discussion on how the existing CAD technology is able to support the proposed flow will close the first part. The second part will focus on RT level and gate level power estimation and optimization techniques, commercially available power management solutions and future directions for industrial low power solutions. The third part will focus on recent power optimization techniques in logical and physical synthesis. The last part of the tutorial will provide an industrial design perspective. It will provide examples of applications of the above tools and techniques to real designs. Both power estimation and power optimization experiments and results will be presented and discussed in detail.



Tutorial 6

Friday, June 22

FIELD PROGRAMMABLE DEVICES: ARCHITECTURE AND CAD TOOLS

rm: N107 - N108

ORGANIZER: *Majid Sarafzadeh* - Univ. of California, Los Angeles, CA
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Alireza Kaviani - Xilinx, Inc., San Jose, CA
Eyal Odiz - Synplicity, Inc., Menlo Park, CA
Majid Sarafzadeh - Univ. of California, Los Angeles, CA

Audience: Architects, CAD tool developer and users of Field Programmable Devices (FPDs). Researchers interested in learning fundamental problems associated with FPDs. Managers interested in learning more about these devices.

Description: Field Programmable Devices (FPDs) represent an exciting technology that is affecting the way digital circuitry is designed. By offering the advantages of faster time to market and ease of design changes, FPDs have become increasingly popular among the designers in both small and large companies. The purpose of this tutorial is to provide an overview of FPD architecture and related CAD techniques in order to provide a clear understanding of both their capabilities and shortcomings.

We start by presenting a short history, starting from the original simple PLAs to today's complex commercial FPDs. After understanding the basics of various FPD architectures we move on to explain more advanced features of recent FPGAs, such as special-purpose circuitry for arithmetic applications, memory blocks, clock management, and I/O features. We demonstrate examples of those features in VirtexII and APEX, which are the most recent products from two of the largest FPD

vendors. Then we look into the near future of commercial products, which involves integrating a microprocessor on FPGAs. The integration of FPGAs and microprocessors on the same chip will potentially expand the current FPD market to embedded systems by creating new applications. In addition, this new product might provide a suitable platform for configurable computing, which requires a successful marriage between two established programmable technologies: reconfigurable hardware and microprocessors. Next, we conclude this part of the tutorial by providing the highlights of the recent academic research efforts dedicated to the architecture of programmable devices with the goal of improving their speed-performance and area-efficiency.

Finally, we review recent synthesis and physical design of FPDs. We review state-of-the-art logic synthesis, technology mapping, placement with wirelength, congestion, and timing optimization followed by routing methodologies. In particular we focus on CAD methodologies that are of interest in dealing with very large FPDs.