



The 39th Design Automation Conference • June 10 - 14, 2002 • New Orleans, LA

Monday, June 10, 2002

	Room 294	Room 293	Room 285	Room 286	Room 288
9:00 - 10:00	Tutorial 1 An Introduction to Embedded Software: Issues, Tools and Methods - for HW and EDA Designers	Hands-On Tutorial Developing Bus-Functional Models for Embedded ATM Switch Verification • SynaptiCAD Inc., Synopsys, Inc.			Introduction to Chips and EDA for a General Audience 10:00 AM - 12:00 PM
12:00	Lunch in Room 296				
1:00 - 2:00	Tutorial 1 (cont.) An Introduction to Embedded Software: Issues, Tools and Methods - for HW and EDA Designers	Hands-On Tutorial Creating and Using a Virtual Prototype for Embedded System Verification • Mentor Graphics Corp., Denali Software, Inc., AXYS Design Automation, Inc., Verisity Design, Inc.	Interoperability Workshop 12:00 PM - 5:00 PM	Workshop for Women in Design Automation: Silk Purses and Sow's Ears: Turning Obstacles into Opportunity 1:15 PM - 4:00 PM	
5:00					

Exhibit Hours 10:00 AM - 6:00 PM / Demo Suite Hours 8:00 AM - 9:00 PM

Hands-On Tutorials (Rooms 293 & 294)

	Monday	Tuesday	Wednesday	Thursday
9:00 - 12:00	Developing Bus-Functional Models for Embedded ATM Switch Verification • SynaptiCAD Inc., Synopsys, Inc.		Hardware-Software Integration on the ARM Wireless PrimeXsys Platform using the CoWare N2C Design System • CoWare, Inc., ARM	Hardware and Software Debug Methods for a Programmable System • Xilinx, Inc., Wind River
2:00 - 5:00	Creating and Using a Virtual Prototype for Embedded System Verification • Mentor Graphics Corp., Denali Software, Inc., AXYS Design Automation, Inc., Verisity Design, Inc.	Assertion-Based Validation with HW/SW for Comprehensive Embedded System Verification • Co-Design Automation, Inc., Real Intent, ARM	Verification of Embedded Communication Systems • Cadence Design Systems, Inc., Xilinx, Inc., Synplicity, Inc.	Top-Level Validation of Complex SoCs • Esterel Technologies

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Tuesday, June 11, 2002

8:30  
to  
10:00

**#** Opening Session and Keynote Speaker **Location: Conference Auditorium**  
**Paradigm Shift in Semiconductor Design: Challenges on the CAD System**  
*Hajime Sasaki* - Chairman of the Board, NEC Corp., Tokyo, Japan

BREAK 10:00 - 10:30					
	<b>Auditorium B</b>	<b>Room 292</b>	<b>Room 288</b>	<b>Room 287</b>	<b>Auditorium A</b>
	Session 1 <b>#</b>	Session 2	Session 3	Session 4	Session 5
10:30 to 12:00	<b>PANEL:</b> Wall Street Evaluates EDA	Web and IP Based Design	Design Innovations for Embedded Processors	Passive Model Order Reduction	New Perspectives in Physical Design
LUNCH 12:00 - 2:00					
	<b>Auditorium B</b>	<b>Auditorium A</b>	<b>Room 292</b>	<b>Room 288</b>	<b>Room 287</b>
	Session 6 <b>#</b>	Session 7	Session 8	Session 9	Session 10
2:00 to 4:00	<b>PANEL:</b> Tools or Users: Which is the Bigger Bottleneck?	<b>SPECIAL SESSION:</b> Life After CMOS: Imminent or Irrelevant?	Formal Verification	High Level Specification and Design	Timing Abstraction
BREAK 4:00 - 4:30					
	Session 11 <b>#</b>	Session 12	Session 13	Session 14	Session 15
4:30 to 6:00	<b>SPECIAL SESSION:</b> E-Textiles	<b>PANEL:</b> Analog Intellectual Property: Now? Or Never?	Low-Power System Design	Fabric-Driven Logic Synthesis	Memory Management and Address Optimization in Embedded Systems

5th SIGDA Ph.D Forum in Room 284 of the Convention Center 6:00 PM - 8:30 PM    **Exhibit Hours** 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM



Videod Sessions

**All Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.**  
 Presenters will be available in room 283 for additional 20-minute question and answer periods after the session.



Wednesday, June 12, 2002

	Auditorium B	Auditorium A	Room 292	Room 288	Room 287
	Session 16	Session 17	Session 18	Session 19	Session 20
8:30 to 10:00	<b>SPECIAL SESSION:</b> Optics: Lighting the Way to EDA Riches?	<b>PANEL:</b> Nanometer Design: What Hurts Next?	Novel DFT, BIST and Diagnosis Techniques	Case Studies In Embedded System Design	Theoretical Foundations of Embedded System Design
BREAK 10:00 - 10:30					
	Session 21	Session 22	Session 23	Session 24	Session 25
10:30 to 12:00	Equivalence Verification	<b>PANEL:</b> Whither (or Wither) ASIC Handoff?	Embedded Software Automation: From Specification to Binary	Applications of Reconfigurable Computing	New Test Methods Targeting Non-Classical Faults
LUNCH 12:00 - 2:00					
	Session 26	Session 27	Session 28	Session 29	Session 30
2:00 to 4:00	<b>SPECIAL SESSION:</b> How Do You Design a 10M Gate ASIC?	Power Distribution Issues	Advances In Synthesis	Analog Synthesis & Design Methodology	Low-Power Physical Design
BREAK 4:00 - 4:30					
	Session 31	Session 32	Session 33	Session 34	Session 35
4:30 to 6:00	<b>PANEL:</b> Unified Tools for SoC Embedded Systems: Mission Critical, Mission Impossible or Mission Irrelevant?	Multi-Voltage, Multi-Threshold Design	Advanced Simulation Techniques	Design Methodologies Meet Network Applications	Advances in Analog Modeling

39th DAC Wednesday Night Carnival Krewe Party • 7:30 PM - 10:30 PM • **Hilton New Orleans Riverside**

**Exhibit Hours** 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

- Videoted Sessions

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Thursday, June 13, 2002

	Auditorium B	Auditorium A	Room 292	Room 288	Room 287
	Session 36	Session 37	Session 38	Session 39	Session 40
8:30 to 10:00	Advances in Timing and Simulation	<b>PANEL:</b> Formal Verification Methods: Getting Around the Brick Wall	Routing and Buffering	System on Chip Design	Timing Analysis and Memory Optimization for Embedded Systems
BREAK 10:00 - 10:30					
	Session 41	Session 42	Session 43	Session 44	Session 45
10:30 to 12:00	Processors and Accelerators For Embedded Applications	<b>PANEL:</b> What is the Next EDA Driver?	Cross-Talk Noise Analysis and Management	Test Cost Reduction for SoCs	Scheduling Techniques for Embedded Systems
Keynote - <i>Software and Silicon - Where's the Equilibrium?</i> • 1:00 - 1:45 • Room: <b>Auditorium B</b> <i>Jerry Fiddler</i> - Chairman and Founder, Wind River					
	Session 46	Session 47	Session 48	Session 49	Session 50
2:00 to 4:00	<b>SPECIAL SESSION:</b> Designing SoCs for Yield Improvement	Advances in SAT	Inductance and Substrate Analysis	Development of Processors and Communication Networks for Embedded Systems	Moving Towards More Effective Validation
BREAK 4:00 - 4:30					
	Session 51	Session 52	Session 53	Session 54	Session 55
4:30 to 6:00	<b>SPECIAL SESSION:</b> Energy Efficient Mobile Computing	Floorplanning and Placement	Circuit Effects in Static Timing	Design Space Exploration for Embedded Systems	Behavioral Synthesis

Demo Suite Hours 8:00 AM - 5:00 PM

- Videoted Sessions

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Friday, June 14, 2002

Tutorials are held at the Ernest N. Morial Convention Center.

8:00 AM - 1:00 PM .....Tutorial Registration Open  
9:00 AM - 5:00 PM .....Tutorials  
8:00 AM .....Continental Breakfast  
12:00 PM .....Lunch (Room 393)

**Tutorial 2 - Intellectual Property Design and Integration for SoCs** rm-291

Organizers: Ralf Seepold - FZI, Karlsruhe, Germany  
Natividad Martínez Madrid - FZI, Karlsruhe, Germany

**Tutorial 3 - Modeling Technology for High Frequency Design** rm-293

Organizer: Joel R. Phillips - Cadence Berkeley Labs., San Jose, CA

**Tutorial 4 - Using SystemC for System Level Modeling and Design** rm-294

Organizers: Kevin Kranen - Synopsys, Inc., Mountain View, CA  
Mike Baird - Willamette HDL, Inc., Beaverton, OR

**Tutorial 5 - Physical Chip Implementation: Hot Spots and Best Practices** rm-295

Organizer: Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA

**Tutorial 6 - New Computing Platforms for Embedded Systems** rm-285

Organizers: Frank Vahid - Univ. of California, Riverside & Center for Embedded Computer Systems, UC Irvine, Irvine, CA  
Walid Najjar - Univ. of California, Riverside, CA

**Topics and Related Sessions**

If you are interested in the following topics, please see the related sessions below.

Embedded Systems:

Sessions: 3, 15, 19, 20, 23, 40, 41, 45, 49, 54

Logic & High Level Synthesis & Optimization:

Sessions: 9, 14, 28, 55

Logic & Functional Verification & Simulation:

Sessions: 8, 21, 33, 37, 47, 50

Timing Verification and Simulation:

Sessions: 10, 36, 53

Electrical, Device & Interconnect Modeling & Simulation:

Sessions: 4, 27, 43, 53

Physical Design:

Sessions: 5, 38, 52

Validation & Test:

Sessions: 18, 25, 44, 46

Impacts of Advancing Technology:

Sessions: 7, 11, 16, 17

Analog and Mixed Signal Design:

Sessions: 12, 29, 35

Low Power Design:

Sessions: 13, 30, 32, 51

Design Re-use, IP and SoC Issues:

Sessions: 2, 24, 31, 39

EDA Methodologies and Industry Issues:

Sessions: 6, 22, 26, 34, 42