



The 40th Design Automation Conference • June 2 - 6, 2003 • Anaheim, CA

Monday, June 2, 2003

	Room 210AB	Room 211AB	Room 210CD	Room 205AB	Room 209AB	Booth #1460
9:00	Tutorial 1	Hands-on Tutorial				DAC Pavilion
10:00	Design Techniques for Power Reduction (Continental Breakfast 8:00 AM - 9:00 AM)	What is All This Noise About Signal and Power Integrity? • Sequence Design, Inc.			Introduction to Chips and EDA For a Non-Technical Audience 10:00AM - 12:00 PM	Managing Mask Costs 10:30 - 11:30
12:00	Lunch					Semiconductor IP Business - Is it Real? 12:00 - 1:00
1:00			Interoperability Workshop 12:00 PM - 5:00 PM	Lunch 1:00PM		
2:00	Tutorial 1 (cont.) Design Techniques for Power Reduction	Hands-on Tutorial Signal and Power Integrity Analysis and Methodology • Synplicity, Inc., Cadence Design Systems, Inc., IOTA Technology Inc.		Workshop for Women in Design Automation: Would Life be Different if Risk Were Not a Factor? Managing Life & Career Transition 2:00 PM - 5:00 PM		
5:00						Ask the CTO 3:00 - 4:00

Exhibit Hours 10:00 AM - 6:00 PM / Demo Suite Hours 8:00 AM - 9:00 PM

Tutorial 1 - Design Techniques for Power Reduction - see pg 36

Hands-on Tutorial - What is All This Noise About Signal and Power Integrity? • Sequence Design, Inc. • see pg 42

Hands-on Tutorial - Signal and Power Integrity Analysis and Methodology • Cadence Design Systems, Inc., IOTA Technology Inc., Synplicity, Inc. • see pg 43

Interoperability Workshop • see pg 41

Workshop for Women in Design Automation • see pg 40

Would Life be Different if Risk Were Not a Factor? Managing Life & Career Transition

Introduction to Chips and EDA For a Non-Technical Audience • see pg 39



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Tuesday, June 3, 2003

- indicates videoed session

8:30
to
10:15

Opening Session and Keynote Speaker Location: Ballroom A-C
<100nm...A Giant Leap for Mankind?
Sir Robin Saxby - Chairman, ARM Holdings plc, Cambridge, UK

BREAK 10:15 - 10:30						
	Ballroom AB	207A-D	210CD	210AB	209AB	Booth #1460
10:30 to 12:00	Session 1	Session 2	Session 3	Session 4	Session 5	DAC Pavilion
	SPECIAL SESSION: Real Challenges and Solutions for Validating Systems-on-Chip	PANEL: Reshaping EDA for Power	Design for Manufacturability and Global Routing	Design Analysis Techniques	Embedded Hardware Design Case Studies	Student Design Contest Awards 11:30 - 12:00
LUNCH 12:00 - 2:00						
2:00 to 4:00	Session 6	Session 7	Session 8	Session 9	Session 10	ARM Twisting: Ask Sir Robin 12:00 - 1:00
	SPECIAL SESSION: Emerging Design and Tool Challenges in RF and Wireless Applications	PANEL: COT - Customer Owned Trouble?	Power Grid Analysis and Optimization	Low-Power Embedded System Design	Cyclic and Non- Cyclic Combinational Circuit Synthesis	EDA Business Forecast Highlights 3:00 - 4:00
BREAK 4:00 - 4:30						
4:30 to 6:30	Session 11	Session 12	Session 13	Session 14	Session 15	
	Managing Leakage Power	PANEL: Emerging Markets: Design Goes Global	Timing-Oriented Placement	Model Order Reduction	Issues in Partitioning and Design Space Exploration for Codesign	

2:00-5:00 Power and Signal
Integrity Modeling and Simulation
of Entire PCBs and IC Packages

SIGDA Ph.D. Forum in Rm. 213A-C from 6:30 PM - 9:00 PM Exhibit Hours 10:00 AM - 6:00 PM / Demo Suite Hours 8:00 AM - 9:00 PM

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.
 Presenters will be available in room 208AB for additional 20-minute question and answer periods after the session.

visit the DAC web site @ www.dac.com for more details



Wednesday, June 4, 2003

Booth #1460	Ballroom AB	207A-D	210CD	210AB	209AB	
DAC Pavilion	Session 16	Session 17	Session 18	Session 19	Session 20	
	SPECIAL SESSION: Nano Technology: Design Implications and CAD Challenges	PANEL: Mixed Signals on Mixed-Signal: The Right Next Technology	Simulation Coverage and Generation for Verification	Tool Support for Architectural Decisions in Embedded Systems	New Topics in Logic Synthesis	8:30 to 10:00
Wall Street's View of EDA - The 2003 Update 10:30 - 11:30	BREAK 10:00 - 10:30					
	Session 21	Session 22	Session 23	Session 24	Session 25	
	SPECIAL SESSION: Coping with Variability: The End of Deterministic Design	PANEL: Cheap Submicron: The Next Implementation Fabric An IEEE D&T Feature Panel	Testbench, Verification and Debugging: Practical Considerations	Delay and Noise Modeling in the Nanometer Regime	Modeling Issues in the Design of Embedded Systems	10:30 to 12:00
	LUNCH 12:00 - 2:00					
Platforms-YES, but What Type is Best? 1:30 - 2:30	Session 26	Session 27	Session 28	Session 29	Session 30	
	SPECIAL SESSION: How Application/ Technology Evolutions will Shape Classical EDA?	SAT and BDD Algorithms for Verification Tools	Elements of Functional and Performance Analysis	Nonlinear Model Order Reduction	Novel Techniques in High-Level Synthesis	2:00 to 4:00
	BREAK 4:00 - 4:30					
	Session 31	Session 32	Session 33	Session 34	Session 35	
	Mixed-Signal Design and Simulation	PANEL: Nanometer Design: Place Your Bets	Novel Self-Test Methods	Technology Mapping, Buffering, and Bus Design	Compilation Techniques for Reconfigurable Devices	4:30 to 6:30

9:00-12:00 Ensuring Signal and Power Integrity at Nanometer Technologies
hands-on

3,125 Gbps With Your Hair on Fire
2:00-5:00
hands-on

Wednesday Night Party • 7:30 PM - 10:00 PM • Disney's California Adventure™ park

Exhibit Hours 10:00 AM - 6:00 PM / Demo Suite Hours 8:00 AM - 9:00 PM

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Thursday, June 5, 2003

- indicates videoed session

	Ballroom AB	207A-D	210CD	210AB	209AB
8:30 to 10:00	Session 36	Session 37	Session 38	Session 39	Session 40
	Architectural Power Estimation and Optimization	PANEL: Libraries: Lifejacket or Straitjacket?	Techniques for Reconfigurable Logic Applications	Test and Diagnosis for Complex Designs	SPECIAL SESSION: Highlights of ISSCC: High-Speed Heterogenous Design Techniques
BREAK 10:00 - 10:30					
10:30 to 12:00	Session 41	Session 42	Session 43	Session 44	Session 45
	SPECIAL SESSION: Highlights of ISSCC and The Design of State-of-the-Art Microprocessors	PANEL: Formal Verification: Prove It or Pitch It	High Frequency Interconnect Modeling	Novel Approaches in Test Cost Reduction	Retargetable Tools for Embedded Software
12:45 - 1:00 • Best Paper Award Presentations Keynote - <i>The Tides of EDA</i> • 1:00 - 1:45 • Room: Ballroom A-C <i>Alberto L. Sangiovanni-Vincentelli</i> - Professor, Univ. of California, Berkeley, CA					
2:00 to 4:00	Session 46	Session 47	Session 48	Session 49	Session 50
	SPECIAL SESSION: ASIC Design in Nanometer Era - Dead or Alive?	Floorplanning and Placement	Advances in SAT	Novel Design Methodologies and Signal Integrity	Memory Optimization for Embedded Systems
BREAK 4:00 - 4:30					
4:30 to 6:00	Session 51	Session 52	Session 53	Session 54	Session 55
	SPECIAL SESSION: Design Automation for Quantum Circuits	Energy-Aware System Design	Budgeting, Simulation and Statistical Timing	Interconnect Noise Avoidance Methodologies and Slew Rate Prediction	Analog Design Space Exploration

Demo Suite Hours 8:00 AM - 5:00 PM

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9:00-12:00 Full-Chip Dynamic Power Grid Methodology From hands-on Planning to Verification

2:00-5:00 Signal and Power Integrity Validation With hands-on In-Circuit Measurements

visit the DAC web site @ www.dac.com for more details



Friday, June 6, 2003

Tutorials are held at the Anaheim Convention Center.

7:30 AM - 6:00 PM.....**Tutorial Registration Open**
8:00 AM**Continental Breakfast**
9:00 AM - 5:00 PM.....**Tutorials**
12:00 PM**Lunch (Room 213A-D)**

Tutorial 2 - SYSTEM-ON-CHIP TEST STRATEGIES

Rm: 205AB

Organizer: **Yervant Zorian** - *Virage Logic Corp., Fremont, CA*

***Tutorial 3 - DESIGN FOR MANUFACTURING
IN THE SUB-100NM ERA***

Rm: 207CD

Organizer: **Louis Scheffer** - *Cadence Design Systems, Inc., San Jose, CA*

Tutorial 4 - ASSERTION-BASED VERIFICATION

Rm: 209AB

Organizer: **Erich Marschner** - *Cadence Design Systems, Inc., Columbia, MD*

***Tutorial 5 - ASSEMBLING AN SOC: COMMUNICATION
ARCHITECTURES AND PROTOCOLS***

Rm: 210AB

Organizer: **Giovanni De Micheli** - *Stanford Univ., Stanford, CA*

Tutorial 6 - HIGH PERFORMANCE ASIC DESIGN

Rm: 210CD

Organizers: **Kurt Keutzer** - *Univ. of California, Berkeley, CA*
David Chinnery - *Univ. of California, Berkeley, CA*

Topics and Related Sessions

If you are interested in the following topics, please see the related sessions below.

Embedded Systems:

Sessions: 5 6 9 15 19 25 28 45 50

Logic & High Level Synthesis & Optimization:

Sessions: 10 15 19 20 30 34

Logic & Functional Verification & Simulation:

Sessions: 1 4 18 23 27 28 42 48

Timing Verification and Simulation:

Sessions: 21 24 41 53

Electrical, Device & Interconnect Modeling & Simulation:

Sessions: 14 24 29 43 49 54

Physical Design:

Sessions: 3 8 13 41 47 54

Validation & Test:

Sessions: 23 33 39 44

Impacts of Advancing Technology:

Sessions: 2 11 16 21 22 26 32 40 41 46 51

Analog and Mixed Signal Design:

Sessions: 17 31 40 49 55

Reconfigurable logic:

Sessions: 35 38 40

Low Power Design:

Sessions: 2 9 11 36 52

Design Re-use, IP and SoC Issues:

Sessions: 1 37

EDA Methodologies and Industry Issues:

Sessions: 1 7 12 26 32 37 46