



Tuesday, June 8, 2004

Speaker Breakfast in Room 1AB at 7:30 AM.

8:30
to
10:00

Opening Session and Keynote Speaker Location: Ballroom 20ABC
Gigascale Integration for Teraops Performance—Challenges, Opportunities and New Frontiers
Patrick P. Gelsinger - Chief Technology Officer & Senior Vice President, Intel Corp.

BREAK 10:00 - 10:30

	Room 6A Session 1	Room 6B Session 2	Room 6C Session 3	Room 6D Session 4	Room 4 Session 5	Booth #3733 DAC Pavilion
10:30 to 12:00	CEO PANEL: EDA: This is Serious Business m/T	SPECIAL SESSION: Management of HOT Leakage m/T	Clock Routing and Buffering m/T	Tools and Strategies for Dynamic Verification m	Timing-Driven System Synthesis m/T	

LUNCH 12:00 - 2:00

	Room 6A Session 6	Room 6B Session 7	Room 6C Session 8	Room 6D Session 9	Room 4 Session 10	Room 6F Session 100	Ask the CTOs: Everything You Ever Wanted to Know But Were Afraid to Ask 2:00 - 2:45
2:00 to 4:00	SPECIAL SESSION: Reliable System-on-a-Chip Design in the Nanometer Era m/T	PANEL: When IC Yield Missed the Target, Who is at Fault? m/T	Power Modeling and Optimization for Embedded Systems T	Performance Evaluation and Run Time Support m/T	Advances in Analog Circuit and Layout Synthesis m/T	BUSINESS DAY: Competitive Strategies for the Electronics Industry	EDA Software Quality 3:00 - 3:45

BREAK 4:00 - 4:30

	Session 11	Session 12	Session 13	Session 14	Session 15	Session 150	Does EDA Need A Roadmap for OS Support 4:00 - 4:45
4:30 to 6:30	Power Grid Design and Analysis Techniques m/T	PANEL: What Happened to ASIC? Go (Recon)figure? m/T	Methods for a Priori Feasible Layout Generation m/T	Abstraction Techniques for Functional Verification T	Memory and Network Optimization in Embedded Designs m/T	BUSINESS DAY: Business Models in IP, Software Licensing, and Services	

SIGDA Ph.D. Forum in Sails Pavilion 6:30 PM - 8:00 PM

Exhibit Hours 9:00 AM - 6:00 PM

Presenters will be available in Room 3 for additional 20-minute question and answer periods after the session.

TOPICAREKEY: ■ Business, ■ Power, ■ Physical/Circuit Design, ■ Nanometer Analysis & Simulation, ■ Logic Design & Test, ■ System Level Design & Verification, ■ Embedded Systems
T = Design Tools Session • **m** = Design Methods Session • **m/T** = Mixed Methods/Tools Session

2:00-5:00 Using Predictive Analysis to Guide Low-Power Design Methodology

Wednesday, June 9, 2004



Speaker Breakfast in Room 1AB at 7:30 AM.

Booth #3733		Room 6A	Room 6B	Room 6C	Room 6D	Room 4	
DRC Pavilion		Session 16	Session 17	Session 18	Session 19	Session 20	
9:00-12:00 Flows for Power Minimization		SPECIAL SESSION: The Future of Timing Closure m/T	PANEL: Verification, What Works and What Doesn't m/T	Design Space Exploration and Scheduling for Embedded Software T	Advances in Accelerated Simulation m	Design for Manufacturability T	8:30 to 10:00
	BREAK 10:00 - 10:30						
hands-on	Standards at the International Level 10:15 - 11:00	Session 21 Statistical Timing Analysis T	Session 22 PANEL: System-Level Design: Six Success Stories in Search of an Industry m/T	Session 23 New Ideas in Placement T	Session 24 Model Order Reduction and Variational Techniques for Parasitic Analysis T	Session 25 Compilation Techniques for Embedded Applications T	10:30 to 12:00
	IP Quality: State-of-the-Art Technical Approaches and Their Business Impacts 11:15 - 12:00	LUNCH 12:00 - 2:00					
2:00-5:00 Structured ASIC / Platform ASIC Design Methodology	Interview with EDA's Woman of the Year 2:00 - 2:45	Session 26 SPECIAL SESSION: Platform-Based System Design m/T	Session 27 Innovations in Logic Synthesis m/T	Session 28 Yield Estimation and Optimization T	Session 29 High-Level Techniques for Signal Processing m/T	Session 30 Advanced Test Solutions T	2:00 to 4:00
	Student Design Contest Award Presentations 3:00 - 3:45	BREAK 4:00 - 4:30					
hands-on		Session 31 Advances in Boolean Analysis Techniques T	Session 32 PANEL: Were the Good Old Days all that Good? EDA Then and Now m/T	Session 33 Power Optimization for Real-Time and Media Rich Embedded Systems m/T	Session 34 Latency Tolerance and Asynchronous Design T	Session 35 New Technologies in System Design m/T	4:30 to 6:30

Exhibit Hours 9:00 AM - 6:00 PM

Wednesday Night Party • 7:30 PM - 10:00 PM • San Diego Marriott Hotel & Marina

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Thursday, June 10, 2004

Speaker Breakfast in Room 1AB at 7:30 AM. • Exhibit Hours 9:00 AM - 6:00 PM

	Room 6A	Room 6B	Room 6C	Room 6D	Room 4	Booth #3733
	Session 36	Session 37	Session 38	Session 39	Session 40	DAC Pavilion
8:30 to 10:00	SPECIAL SESSION: BioMEMS M/T	PANEL: Will Moore's Law Rule in the Land of Analog? M/T	Floorplanning T	Issues in Timing Analysis T	SPECIAL SESSION: ISSCC Highlights M/T	ASIC, COT, or FPGA: Which Should Your Next Chip Be? 10:15 - 11:00
BREAK 10:00 - 10:30						
	Session 41	Session 42	Session 43	Session 44	Session 45	ASIC, COT, or FPGA: Which Should Your Next Chip Be? 10:15 - 11:00
10:30 to 12:00	SPECIAL SESSION: Multiprocessor SoC MPSoC Solutions/ Nightmare M/T	PANEL: Is Statistical Timing Statistically Significant? M/T	Timing Issues in Placement M/T	Design Methodologies for ASIPs M	FPGA-Based Systems M	
Keynote - EDA Industry Growth - Are There Enough New Problems to Solve? • 12:45 - 1:45 • Ballroom 20ABC Walden C. Rhines - Chairman EDA Consortium, CEO and Chairman, Mentoptr Graphics Corp. Best Paper Award Presentations						9:00-12:00 Physical Design of Structured ASICs 2:00-5:00 Designing a Structured ASIC through FPGA Prototyping hands-on hands-on
	Session 46	Session 47	Session 48	Session 49	Session 50	
2:00 to 4:00	SPECIAL SESSION: Security as a New Dimension in Embedded System Design M/T	Leakage Power Optimization M/T	Interconnect Extraction M/T	New Frontiers in Logic Synthesis T	Numerical Techniques for Simulation M/T	
BREAK 4:00 - 4:30						
	Session 51	Session 52	Session 53	Session 54	Session 55	
4:30 to 6:00	Energy and Thermal-Aware Design M	Noise-Tolerant Design and Analysis Techniques M/T	New Tools and Methods for Future Embedded SoC M/T	New Scan-Based Test Techniques M/T	CAD for Reconfigurable Computing M/T	

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Friday, June 11, 2004



Tutorials are held at the San Diego Convention Center .

7:00 AM - 6:00 PMTutorial Registration Open
8:00 AMContinental Breakfast
9:00 AM - 5:00 PMTutorials
12:00 PMLunch (Rm: 6A)

Tutorial 2 - AUTOMATED MACROMODELLING TECHNIQUES FOR DESIGN OF COMPLEX ANALOG, MIXED-SIGNAL INTEGRATED SYSTEMS
Rm: 1AB

Organizer: Jaijeet Roychowdhury - Univ. of Minnesota, Minneapolis, MN

Tutorial 3 - BUFFERING INTERCONNECT: FROM BASICS TO BREAKTHROUGHS
Rm: 6B

Organizer: Weiping Shi - Texas A&M Univ., College Station, TX

Tutorial 4 - LINUX FOR REAL-TIME AND EMBEDDED SYSTEMS
Rm: 4

Organizer: Marco Di Natale - ReTis Lab. Scuola Superiore S. Anna, Pisa, Italy

Tutorial 5 - SILICON DEBUG - WHAT DO YOU DO WHEN YOUR ASIC DOES NOT WORK AS FAST AS EXPECTED?
Rm: 6C

Organizer: Doug Josephson - Hewlett-Packard, Fort Collins, CO

Tutorial 6 - SYSTEMVERILOG FOR VERIFICATION: THE UNIFICATION OF DESIGN, TESTBENCH AND ASSERTIONS IN A SINGLE LANGUAGE
Rm: 6D

Organizer: Tom Fitzpatrick - Synopsys, Inc., Marlboro, MA
Topics and Related Sessions

If you are interested in the following topics, please see the related sessions below.

Business:

■ Sessions: 1, 7, 100, 12, 150, 32

Power:

■ Sessions: 2, 6, 8, 11, 33, 40, 47, 51

Physical/Circuit Design:

■ Sessions: 3, 10, 13, 16, 23, 37, 38, 43, 50

Nanometer Analysis & Simulation:

■ Sessions: 20, 21, 24, 28, 36, 39, 42, 48, 52

Logic Design & Test:

■ Sessions: 27, 30, 34, 45, 49, 54, 55

System Level Design & Verification:

■ Sessions: 4, 5, 14, 17, 19, 22, 26, 29, 31, 35, 41, 46

Embedded Systems:

■ Sessions: 9, 15, 18, 25, 44, 53