

The 43rd Design Automation Conference • July 24 - 28, 2006 • San Francisco, CA

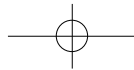


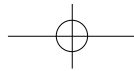
Monday, July 24

	Rm: 305	Rm: 304	Rm: 309	Rm: 303	Rm: 302	Rm: 301	Booth #2228
9:00	Tutorial 1 ESL Design Methodology Using SystemC (Breakfast 8:00 am - 9:00 am in Rm: 306/308)	Tutorial 2 Practical Aspects of Coping with Variability: An Electrical View (Breakfast 8:00 am - 9:00 am in Rm: 306/308)	Hands-on Tutorial Analysis and Optimization of Low Power Designs <i>Apache Design Solutions</i>		Workshop for Women in Design Automation 9:00 am – 12:45 pm	Introduction to Chips and EDA for a Non-Technical Audience 10:00 am - 12:00 pm	DAC Pavilion
10:00							
12:00	Lunch (Rm: 306/308)	Lunch (Rm: 306/308)					What Will it Take to Break the \$4B Revenue Cap? 11:00 am - 12:00 pm
1:00	Tutorial 1 (cont.) ESL Design Methodology Using SystemC	Tutorial 2 (cont.) Practical Aspects of Coping with Variability: An Electrical View	Rm: 310 Hands-on Tutorial Using Virtual System Prototypes to Optimize Architectures for Low Power and Other Key Attributes <i>VaST, StarCore</i>	Second Integrated Design System Workshop: How Can We Solve the Challenges of Design System Integration 12:00 pm - 5:00 pm	Lunch: 12:45 pm – 1:45 pm		Ask the CTO 1:00 pm - 2:00 pm
2:00							
5:00	📣 2:00 pm • Gateway Ballroom • Keynote - iPod or Iridium - Which One are You Going to Be? Joe Costello - Chairman of the Board, Orb Networks, Inc.						Mass Book Signing 4:15 pm - 5:15 pm

IEEE CEDA Reception and Distinguished Speaker Lecture in Rm: 124 from 5:30 pm - 7:30 pm

📣 - Indicates videoed session 📌 - Indicates special interest to designers • Presenters will be available in room 310 for additional 20-minute question-and-answer periods after the session.
Session Tracks: ■ Business ■ System Level and Embedded ■ MEGa ■ Low Power and Power ■ Analog and Circuit ■ Interconnect, Reliability and DFM ■ Verification and Test ■ Synthesis and FPGA ■ Physical Design ■ Beyond the Die ■ New and Emerging Technologies





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Tuesday, July 25

8:30
to
10:15

General Session and Keynote Speaker Gateway Ballroom
Structuring Process and Design for Future Mobile Communication Devices
Hans Stork - Senior Vice President and Chief Technology Officer, Director of Silicon Technology Department, Texas Instruments Inc.

BREAK 10:15am - 10:30am

10:30
to
12:00

306/308	307	305	304	303
Session 1	Session 2	Session 3	Session 4	Session 5
FABLESS PANEL: How will the Fabless Model Survive?	SPECIAL SESSION: Why Doesn't My System Work?	Hierarchical Synthesis for Mixed-Signal Designs	Processor and Communication Centric SoC Design	Practical Applications for DFM

Booth #2228
DAC Pavilion
The Do's and Don'ts of Verification 10:15 am - 11:00 am

LUNCH 12:00pm - 2:00pm

2:00
to
4:00

306/308	307	305	304	303	301
Session 6	Session 7	Session 8	Session 9	Session 10	Session 100
PANEL: The IC Nanometer Race: What Will it Take to Win?	SPECIAL SESSION: Bridging the System to RTL Verification Gap	Leakage, Power Analysis and Optimization	MPSoC Design Methodologies and Applications	Statistical Timing Analysis	MANAGEMENT: Decision-Making for Complex SoCs in Consumer Electronic Products

Design Team Collaboration: Tools Challenge or Organization Responsibility 11:30 am - 12:15 pm
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Exporting in the Hallway 1:00 pm - 1:45 pm

Shattering the Glass Ceiling: A Decade of Growth for Women 2:00 pm - 2:45 pm

BREAK 4:00pm - 4:30pm

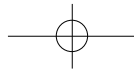
4:30
to
6:30

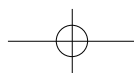
Session 11	Session 12	Session 13	Session 14	Session 15	Session 150
PANEL: Entering the Hot Zone - Can You Handle the Heat and Be Cool?	SPECIAL SESSION: Reliability Challenges for 65nm and Beyond	Power Grid Analysis and Design	Advances in Formal Solvers	Gate Modeling and Model Order Reduction	MANAGEMENT: Tradeoffs and Choices for Emerging SoCs in High-End Applications

The Fabless Model: Is DFM Our Salvation or Demise? 4:00 pm - 4:45 pm

SIGDA Ph.D. Forum and Member Meeting in Rm 310 from 6:30pm - 8:00pm

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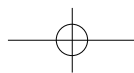
Wednesday, July 26

	306/308	307	305	304	303	301	Booth #2228
	Session 16	Session 17	Session 18	Session 19	Session 20	Session 21	DAC Pavilion
8:30 to 10:00	SPECIAL SESSION: MPSoC Design Tools	SPECIAL SESSION: Highlights of ISSCC: Multimedia	Buffer Insertion	Testing and Validation for Timing Defects	Advanced Topics in Processor and System Verification	Software for Real-Time Applications	
BREAK 10:00am - 10:30am							
	Session 22	Session 23	Session 24	Session 25	Session 26	Session 27	Student Design Contest Award Presentations 10:00am - 10:45am
10:30 to 12:00	PANEL: Building a Standard ESL Design and Verification Methodology: Is it Just a Dream?	INVITED SESSION: CAD Challenges for Leading-Edge Multimedia Designs	Routing	The Test Bin	PANEL: Variation- Aware Analysis: Savior for the Nanometer Era?	Low Power and Ultra- Low Voltage Design	The Xbox 360 Unlocked: Doing What it Takes to Get Chips into High-Volume Consumer Electronics 11:15 am - 12:00 pm
LUNCH 12:00pm - 2:00pm							
	Session 28	Session 29	Session 30	Session 31	Session 32	Session 33	AMD/DreamWorks - Fueling Technology Innovation 1:00 pm - 2:00 pm
2:00 to 4:00	High-Level Exploration and Optimization	PANEL: Design Challenges for Next- Generation Multimedia, Games, and Entertainment Platforms	CAD for FPGAs	Secure Systems	Logic Synthesis I	Low-Power, Thermal Aware Architectures	ESL: Software Engineers are from Pluto and Hardware Engineers are from Mercury: Can ESL bridge the gap? 2:15 pm - 3:15 pm
BREAK 4:00pm - 4:30pm							
	Session 34	Session 35	Session 36	Session 37	Session 38	Session 39	The Accidental Pirate 4:00 pm - 4:45 pm
4:30 to 6:30	Low Power System Level Design	Power-Constrained Design for Multimedia	Electrical and Thermal Issues in FPGAs	SPECIAL SESSION: Beyond Low Power Design: Environmental Energy Harvesting	Communication Driven Synthesis	Parallelism and Memory Optimizations	

Wednesday Night Party • 7:30pm - 10:00pm • AT&T Ballpark

- Indicates videod session
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Session Tracks:
■ Business
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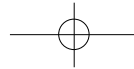
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Thursday, July 27

	306/308	307	305	304	303	301	Booth #2228
8:30 to 10:00	Session 40 PANEL: Tomorrow's Analog: Just Dead or Just Different?	Session 41 🗣️ Nanotubes and Nanowires	Session 42 Simulation Assisted Formal Verification	Session 43 Yield Analysis and Improvement	Session 44 Approaches to Soft Error Mitigation	Session 45 Design/Technology Interaction	DAC Pavilion
BREAK 10:00am - 10:30am							
10:30 to 12:00	Session 46 PANEL: Building a Verification Test Plan: Trading Brute Force for Finesse	Session 47 🗣️ SPECIAL SESSION: More Moore's Law and More than Moore's Law	Session 48 Formal Specification and Verification Testbench Generation	Session 49 Analysis and Optimization Issues in NoC Design	Session 50 SPECIAL SESSION: Key Technologies for Beyond the Die	Session 51 Analog Design and Design Assistance	Developing Consumer SoCs - IP and Automation or Sticks and Duct Tape 10:00 am - 10:45 am
🗣️ 12:45pm - 1:45pm • Gateway Ballroom • Award Presentations and Keynote - The Challenges of Convergence <i>Alessandro Cremonesi</i> - Strategy and System Technology Group Vice-President and Advanced System Technology General Manager, STMicroelectronics							
2:00 to 4:00	Session 52 High Performance Simulation of Transaction Level and Dataflow Models	Session 53 🗣️ Nano- and Bio-Chip Design	Session 54 Logic and Sequential Synthesis	Session 55 Low Power Circuit Design	Session 56 Beyond-the-Die Circuit and System Integration	Session 57 New Ideas in Analog/RF Modeling and Simulation	Wireless USB - The Next Ubiquitous Connectivity Standard? 11:00 am - 11:45 am
BREAK 4:00pm - 4:30pm							
4:30 to 6:30	Session 58 Advanced Methods for Interconnect Extraction, Clocks and Reliability	Session 59 🗣️ PANEL: DFM: Where's the Proof of Value?	Session 60 Bounded Model Checking and Equivalence Verification	Session 61 Test Response Compaction and ATPG	Session 62 Placement		Troubleshooting the Multi-Processor SoC Design Flow 12:00 pm - 12:45 pm

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Session Tracks: 🗣️ **Business** 🗣️ **System Level and Embedded** 🗣️ **MEGA** 🗣️ **Low Power and Power** 🗣️ **Analog and Circuit** 🗣️ **Interconnect, Reliability and DFM** 🗣️ **Verification and Test** 🗣️ **Synthesis and FPGA** 🗣️ **Physical Design** 🗣️ **Beyond the Die** 🗣️ **New and Emerging Technologies**



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Friday, July 28

TUTORIAL 3 - REAL DFM SOLUTIONS - TOOLS, METHODOLOGIES, AND SUCCESSES

Rm: 304

Organizer: **Andrew B. Kahng** - Univ. of California at San Diego, La Jolla, CA
Presenters: **Nagaraj NS** - Texas Instruments Inc., Dallas, TX
Jean-Pierre Schoellkopf - STMicroelectronics, Crolles, France
Mike Smayling - Applied Materials, Sunnyvale, CA
Ban P. Wong - Chartered Semiconductor, Milpitas, CA
Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA

TUTORIAL 4 - SURVIVING AND THRIVING IN THE WORLD OF CHIP AND PACKAGE CO-DESIGN

Rm: 305

Organizers: **Chung-Kuan Cheng** - Univ. of California at San Diego, La Jolla, CA
Howard Chen - IBM Corp., Yorktown Heights, NY
Presenters: **Paul Harvey** - IBM Corp., Austin, TX
Howard Chen - IBM Corp., Yorktown Heights, NY
Lei He - Univ. of California, Los Angeles, CA
Chung-Kuan Cheng - Univ. of California at San Diego, La Jolla, CA
Kaushik Sheth - Rio Design Automation, Inc., Santa Clara, CA

TUTORIAL 5 - SYSTEMVERILOG: LANGUAGE TUTORIAL AND INDUSTRIAL VERIFICATION EXPERIENCE

Rm: 307

Organizer: **Johny Srouji** - IBM Corp., Austin, TX
Presenters: **Johny Srouji** - IBM Corp., Austin, TX
Karen Pieper - Synopsys, Inc., Sunnyvale, CA
Tom Fitzpatrick - Mentor Graphics Corp., Groton, MA
John Havlicek - Freescale Semiconductor, Inc., Austin, TX
Matt Maidment - Intel Corp., Portland, OR
Cliff Cummings - Sunburst Design, Inc., Portland, OR

TUTORIAL 6 - TOOLS FOR HYBRID EMBEDDED SYSTEMS: MODELING, VERIFICATION, AND DESIGN

Rm: 302

Organizer: **Luca Carloni** - Columbia Univ., New York, NY
Presenters: **Hilding Elmqvist** - Dynasim AB, Lund, Sweden
George Pappas - Univ. of Pennsylvania, Philadelphia, PA
Pieter J. Mosterman - The MathWorks, Inc., Natick, MA
Alessandro Pinto - Univ. of California, Berkeley, CA
Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

TUTORIAL 7 - FROM BASIC TO ADVANCED TECHNIQUES FOR SILICON DEBUG AND DIAGNOSIS

Rm: 306/308

Organizer: **Srikanth Venkataraman** - Intel Corp., Hillsboro, OR
Presenters: **Srikanth Venkataraman** - Intel Corp., Hillsboro, OR
Miron Abramovici - DAFCA Inc., Framingham, MA
Robert Aitken - ARM, Sunnyvale, CA

